Fabrication of Nanoscale Artificial Synapses of Halide Perovskite

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Abstract

This research explored the immense potential of halide perovskite to be used in the field of neuromorphic computing. Due to their mixed ionic-electronic conduction, halide perovskites offer a unique opportunity to revolutionize future computing technologies by developing novel memristors with unprecedented data storage density.

This work focused on the fabrication of artificial synapses, that mimic the behaviour of the human nervous system, with a key emphasis on extremely low energy consumption per event of resistance switching. The objective was to create synapses that are as energy-efficient as their biological equivalents, achieving energy consumption levels below 100 fJ per event. To execute this, nanofabrication techniques were employed to pattern micro- and nanostructures in which perovskite was grown.

The step-by-step fabrication route of an artificial synapse was established, with successful confinement of $MAPbI_3$ crystals, within 5-µm holes. The structural and optical analysis of obtained samples was conducted through scanning electron microscopy (SEM), optical microscopy, and optical spectroscopy. Subsequently, the electronic properties of the final device were measured to assess its data storage capabilities. While hysteresis is yet to be observed, the electronic behaviour of the samples, featuring notably low current values, indicates that further optimization of the method holds the key to unlocking the full potential of these innovative devices.

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Introduction

Halide perovskites form a group of materials that exhibit huge potential to be incorporated in a vast majority of optoelectronic devices including lasers, solar panels and light-emitting diodes [1, 2]. What is more, they are not only excellent conductors of electronic charges but also outstanding conductors of ions [3–5]. Due to the intrinsic current-voltage hysteresis, arising from different mobility of electronic and ionic charge carriers, these materials emerged as prospects for completely groundbreaking applications, far above the range of conventional semiconductors [6, 7].

Neuromorphic computing is an example of a scientific field that can profit from utilizing halide perovskites [8]. The ability to reversibly tune the resistance of the perovskite material paves the way to make memristors from them which would be characterized by data storage density of unprecedented capacity [8–10].

In this work, a novel type of memristor called an artificial synapse, emulating the behaviour of the human nervous system, will be made. The key property of artificial synapses is their extremely low energy consumption per event of resistance switching [1]. Therefore, one of the goals of the research was to fabricate synapses with a memory imprinting as energy-efficient as their biological equivalents ($>$100 fJ/per event) [11]. Knowing that the energy consumption scales with the device area [3], the idea was to use nanofabrication tools to pattern structures in which perovskite will be grown.

The step-by-step fabrication procedure of an artificial synapse was established. The growth of hybrid organic-inorganic halide perovskite crystals, namely $MAPbI_3$, was successfully confined to the 5-µm holes, leaving room for further downscaling. The structural and optical analysis of $MAPbI_3$ crystals was performed using SEM, optical microscopy, and optical spectroscopy. Finally, the electronic properties of the final device were measured to establish if it serves its data storage purpose. Although the hysteresis was not observed so far, the electronic behaviour of the samples, that is, very low current values, suggests that it is mostly an issue of optimization to harvest the full potential of the device.

Theory

This section provides the theoretical background necessary to understand the objectives and results of the project.

2.1 Memristors

A memristor (memory + resistor) is a 2 or 3-terminal electrical component whose resistance can be modulated by the external electric field [4, 6]. The ability of a memristor to reversibly change its conductance is often exploited for memory storage purposes [2, 4]. Due to the remarkable properties of the final device such as ultra-low energy consumption, the possibility to downscale, and fast switching speeds, a memristor is anticipated to emerge as a novel foundational component for electronics [2, 12]. It is mostly built in a sandwich-like architecture in which a semiconductor or an insulator is inserted between two metal electrodes [9, 13]. The ionic charge transport in the active layer between two electrodes allows for information storage due to the resistive switching (RS) mechanism between different resistance states [2]. There might be multiple resistance states in a single memristor but in nomenclature, the high resistance state (HRS) and low resistance state (LRS) are always distinguished and the degree of resistance change between them validates the functionality of the memristor [10]. In principle, the device conductivity remains the same until a certain voltage threshold is reached which triggers the transition from HRS to LRS. A reverse voltage sweep is needed to go back to the initial LRS state [14, 15]. Hence the memory storage is based on the temporary local structural changes in the semiconductor sandwiched between the top and bottom contacts [4]. The electrical properties of a memristor arise from its current-voltage behaviour, which shows hysteresis (Fig. 2.1). In many applications, the hysteresis has a detrimental effect on the performance, whereas for memristors it is exploited and even magnified to achieve higher levels of switching [12].

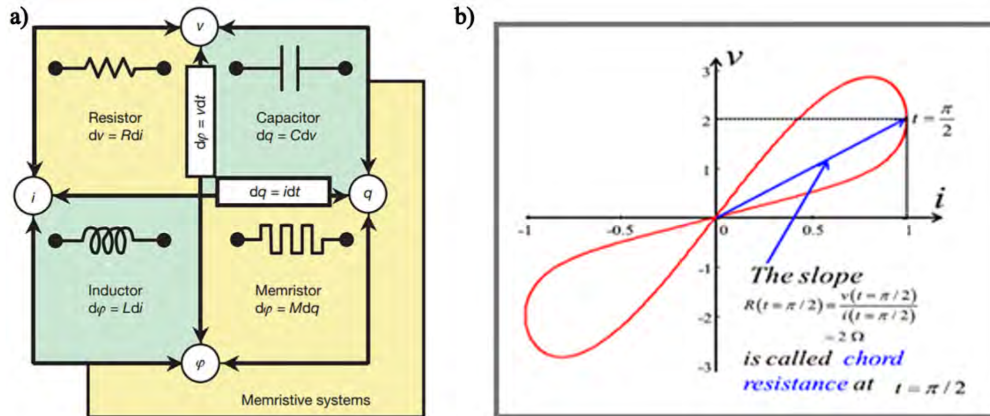


Figure 2.1: Characteristics of a memristor. **a)** Division of fundamental electrical components. **b)** Theoretical I-V hysteresis loop of Hewlett Packard's memristors [21]. Images taken from [2].

2.1.1 Artificial synapses

The phenomenon responsible for learning and remembering in the human nervous system is called synaptic plasticity [3, 16]. It is related to the tunable change of the synaptic weight while receiving electrical stimuli from the brain [17]. Once the stimulation stops the synapse gradually returns to its initial state, thus the process is reversible [12]. It is visible that there are a lot of links tying synaptic and memristive behaviour together. They were a building block for the development of the new type of memristors known as artificial synapses, that try to resemble the actual brain functions [2, 7]. With the energy consumption being equivalent to its biological analogues (around 10 fJ per event) they offer a clear perspective to utilize them in brain-inspired computing [1, 18]. The structure of memristors mimics one of the brain synapses, where the top electrode, semiconductor and bottom electrode correspond to the presynaptic membrane, synaptic cleft and postsynaptic membrane, respectively (Fig. 2.2) [19]. Therefore, the top electrode is the one experiencing the external stimulus, forcing the ionic charge carriers in the semiconductor layer to dislocate, consequently influencing the overall conductivity of the device [16, 20]. The difference in readout current on the bottom electrode provides information on the magnitude of the device's resistance change.

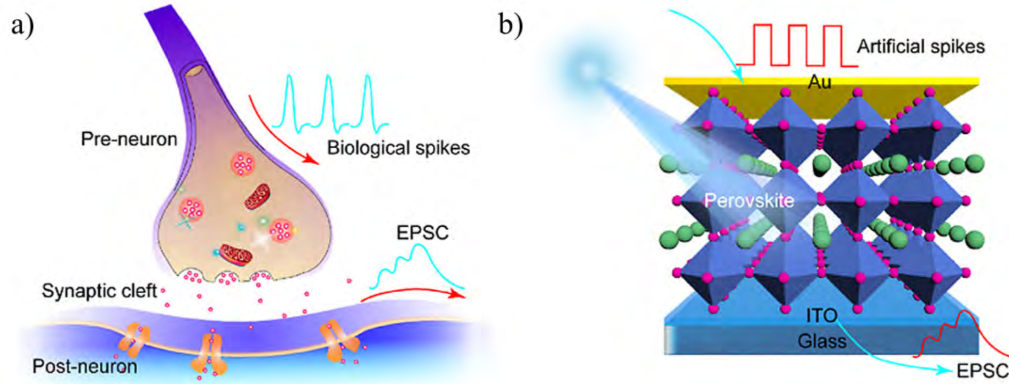


Figure 2.2: Analogies between biological and artificial synapses. **a)** A visual representation of a brain synapse. **b)** Working principle and the structure of the artificial synapse based on halide perovskite. EPSC stands for the excitatory postsynaptic current which in a biological nomenclature causes and stimulates the neural response. Images taken from [19].

2.1.2 Perovskites for artificial synapses

Initial artificial synapses were obtained using CMOS chips with complicated circuit configurations which limited the main objective of lowering energy consumption [1]. In order to make such a memristor, many different functional materials were then investigated, ranging from chalcogenides to organic materials [2]. Recently, perovskites emerged as a potential breakthrough material for this memory storage application. Their tunable bandgap, easily induced ion migration and light sensitivity provided enough motivation to give them an in-depth examination [7, 19]. A particular interest was put in the hybrid organic-inorganic halide perovskites because they combine the advantages of both organic and inorganic equivalents and offer an even higher degree of properties tunability [2]. Such semiconductor materials, e.g. $MAPbI_3$, have very low activation energy for the ion migration, a high defect density and exhibit mixed ionic-electronic conduction [2, 9]. Due to the latter one, they show intrinsic hysteresis, which allows them to effectively fulfil the working requirements of artificial synapses, whereas low activation energy of ion migration signifies the ability to consume a very low amount of energy per operation [10, 20, 22].

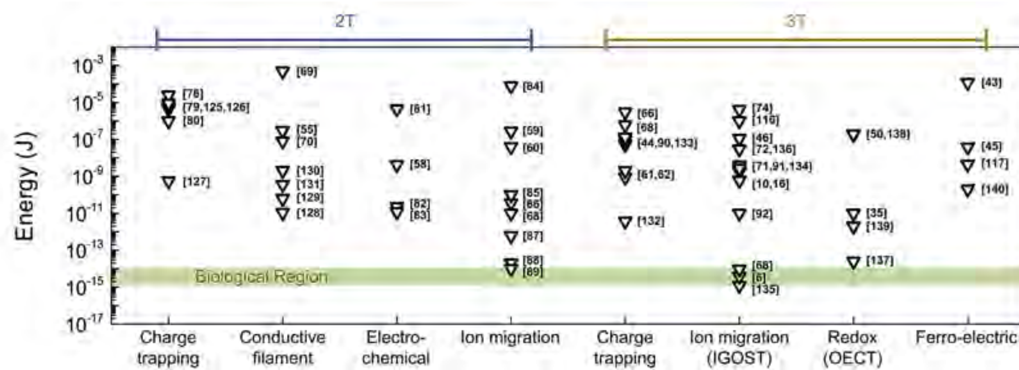


Figure 2.3: Overview of energy consumption for organic artificial synapses based on their structure and operating mechanism. Image taken from [11].

2.1.3 Energy consumption

Artificial synapses vary from each other in their properties depending on the chosen active material, the size of the device, and the designed device architecture [11]. The ultra-low power and energy consumption are vital conditions to create brain-inspired computing systems based on artificial synapses [17]. The final device should produce a sensitive response to the weakest possible stimuli and be able to enhance it to the highest possible degree. It is very important to indicate that energy consumption scales with the size of the device, thereby by making the memristor smaller, we can effectively lower the amount of energy used per switching event [3, 11, 22]. The power P [W] of the device is characterized by the following equation 2.1

$$P = I \cdot V \tag{2.1}$$

where I [A] is the current and V [V] is the voltage. To calculate the energy consumption E [J] in the simplified case where I and t are at their maximum, one can use the equation 2.2

$$E = P \cdot t \tag{2.2}$$

where P [W] is the power and t [s] is the time [11]. Fig. 2.3 provides the range of energy consumption for both 2 and 3 terminal devices made with different approaches [11]. Some works have already created artificial synapses with the magnitude of energy consumption respective to the biological ones, utilizing,

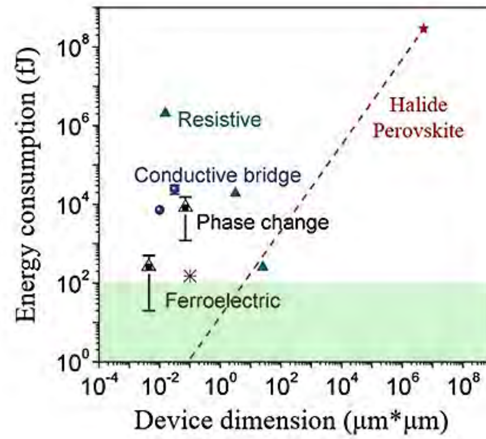


Figure 2.4: Comparison of energy consumption of different synaptic devices. The red dashed line indicates how the decrease in size of the device based on halide perovskite should affect its energy consumption (assuming that the poling current scales linearly with the area of the device). The green rectangle highlights the range of energy consumption for artificial synapses. Image recreated from [3].

e.g. electrolyte-gated vertical organic transistors [18]. Many research groups are currently working to get such results with the perovskite as an active layer. Judging by the results obtained by Xiao and Huang [3] the device made with a halide perovskite with an area of around 10 μm^2 should already be in the desired order of energy consumption of tens of femtojoules (Fig. 2.4).

2.2 Patterning of the perovskite

It is known that one of the approaches to lower the energy consumption of artificial synapses is to lower the size of the device [3, 22]. Not only the field of neuromorphic computing could benefit from this but also many different optoelectronic applications such as solar cells or photodetectors [23, 24]. On this basis, a lot of effort was placed into attempts to downscale the devices made of halide perovskite to the nanoscale and pattern them in the desired fashion [25]. Finding a perfect method to do it is the holy grail among perovskite researchers since it would further improve the properties of the perovskite in comparison to its bulk form [24]. For instance, many

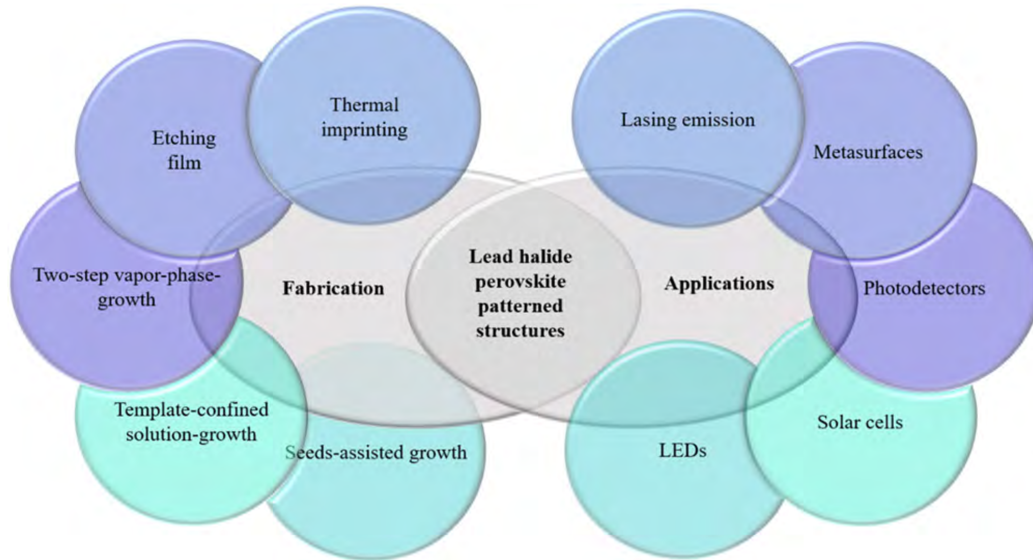


Figure 2.5: Summary of fabrication methods and applications of lead halide perovskite patterned structures. Image taken from [24].

enhanced or even novel properties could be programmed by taking advantage of light-scattering effects if one could have control over the spatial distribution of perovskite crystals. There are several established ways to pattern the perovskite into organized arrays (Fig. 2.5) but each technique faces specific problems that downgrade the functional properties of the device [23, 24].

2.2.1 Techniques

The techniques to pattern the perovskite can be generally divided into two groups: top-down and bottom-up.

Top-down methods

Top-down methods rely on the processing of the perovskite thin film that was deposited on the given substrate, with thermal imprinting and etching film being examples of such an approach [23]. To imprint the desired pattern on the film one needs a mechanical mold or form with a fabricated inverse pattern. Application of the form with a set pressure to the perovskite film and simultaneously heating it results in a reliably patterned structure, what

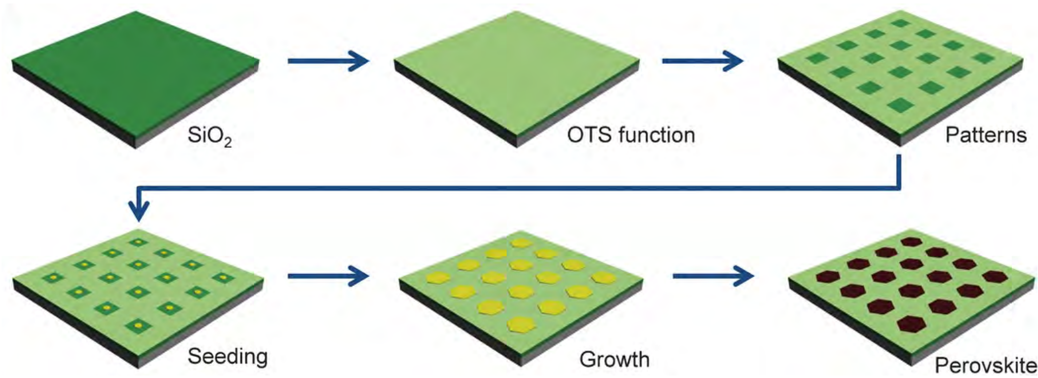


Figure 2.6: Fabrication route to obtain the $MAPbI_3$ microplate crystals established by Wang et al. that inspired the approach used in this work. Image taken from [29].

was confirmed by both Pourdavoud et al. and Kamminga et al. [26, 27]. In the case of etching a certain template, e.g. a photoresist, has to be placed over the perovskite film to block the incoming plasma or ion beam used to print the patterns in the perovskite material. For instance, Gao and the other authors designed their own templates and by adjusting their periodicity they varied the periodicity of the patterned perovskite gratings too [28]. This method offers a nice alternative to the imprinting one because it does not require any external pressure and elevated temperatures.

Bottom-up methods

Bottom-up methods are less mechanical than top-down methods as they utilize the direct growth of perovskite crystals in the designed pattern or inside the pre-patterned structures. These techniques try to design chemical reactions between reagents or exploit the differences in the water affinity of given layers to confine the perovskite to a certain location on the sample [30]. Wang et al. variation of the two-step vapour-phase-growth (Fig. 2.6) took advantage of both these aspects. The transition of PbI_2 to $MAPbI_3$ from the MAI vapour was improved by the silanization of the SiO_2 surface which limited the growth of the PbI_2 seeds to the desired places on the substrate [29, 31]. He with his partners used surface silanization as well to ensure that the perovskite precursor will end up in the designated spots but they also

used a patterned PDMS mold to confine the growth of the perovskite in a vertical direction, therefore getting more control over the general dimensions of its crystals. [32]

2.2.2 Limitations

The biggest and most general difficulty in patterning perovskites comes from their low stability and high solubility in many solvents which makes them incompatible with photolithography [25, 30]. Aside from that each method experiences its specific problems. For example, top-down techniques struggle with material losses as the methods are very mechanical. On top of that, the processes such as etching have destructive effects on the quality of perovskite crystals. On the other hand, it is a challenge to control the morphology of crystals with the bottom-up methods. The uniformity of the particular crystals is also very tough to maintain with these techniques. The ones that implement templates in the manufacturing procedure can waste some material as well [24].

Summary

Due to the exceptional electronic properties of $MAPbI_3$ which match the requirements of a memristor, we aim to manufacture artificial synapses with this material sandwiched between the bottom and top electrode. To get the lowest-possible energy consumption for our artificial synapses we decided to downscale the dimensions of the perovskite by placing it into patterned micro- and nanoholes. The bottom-up method established by Wang et al. [29] inspired us to create periodic structures on the samples which differ in the degree of surface wettability. This way we could confine the growth of the perovskite crystal to the prepatterned microholes, with a higher affinity for perovskite precursor solution. The top-down methods using mechanical mold helped us to improve the technique by adding external pressure which ensured that the perovskite would only grow in holes.

Materials and Methods

The goal of this section is to help the researchers in future attempts to replicate the results. All materials utilized in this work will be written down with details necessary to ensure the reproducibility of the established procedure. Followingly, the equipment used to perform each step will be catalogued with a list of crucial parameters needed to get the optimized layer thicknesses.

3.1 Materials

A variety of organic and inorganic materials from perovskites to polymers were utilized in order to create an artificial synapse of architecture congruent with the desired properties.

3.1.1 Sample preparation

The 10 cm wide silicon wafer from Siegert Wafer of 525 µm thickness was used as a substrate, on which other layers were deposited. Indium tin oxide (ITO) was used as a bottom electrode. Silicon dioxide (SiO_2) was used as a spacer layer in which the holes were subsequently patterned. Octadecyltricholorosilane (OTS) from Sigma-Aldrich of $\geq$90% purity was used to increase the hydrophobicity of the SiO_2 surface. The top electrode was made of gold (Au).

The solution of positive resist CSAR 62 (AR-P 6200.09) from Allresist with anisole (Honeywell, $>$99%) in a 1:1 ratio was employed for E-beam lithography, whereas for UV-Mask a negative MICROPOSIT S1813 G2 series resist was used. A solution of 50 nm gold colloids from BBInternational placed on a wafer helped to align it with the stage of Voyager. The chemicals used to develop patterned features after e-beam patterning were n-amyl acetate (Thermo Scientific Chemicals, 99%), o-xylene (VWR International BV), methyl isobutyl ketone (VWR International BV) and isopropanol (Biosolve). The development of structures after UV patterning was done with MICROPOSIT MF-319 Developer, containing TMAH. Acetone and isopropanol from Biosolve were frequently utilized in cleaning the wafers and samples.

3.1.2 Perovskite precursor

The substrates in the powder form used to obtain methylammonium lead iodide ($MAPbI_3$) were: methylammonium iodide (MAI) from the company Solaronix and lead iodide (PbI_2) from the company TCI of $>98\%$ purity. Both iodides were then dissolved in dimethylformamide (DMF).

3.2 Equipment and Methods

The fabrication of nanoscale artificial synapses requires the implementation of the same equipment that is conventionally used to construct solar cells. Various lithography, PVD, and CVD techniques were utilized to get smooth layers of a particular material with good adhesion to the compound underneath and thickness on the order of 10^{-8} m.

3.2.1 Fabrication

ITO deposition

The active layer of ITO was deposited on the initial Si substrate with the use of the Sputter PVD system Polyteknik S-Flex. The sputtering chamber was filled entirely with argon since the addition of a different gas, mainly oxygen, would result in lower conductivity of the ITO layer [33]. The gas pressure during sputtering was $5e^{-3}$ mbar. The wafer in the chamber was preheated to 400°C. The actual sputtering step took 900 s using Bipolar DC mode with 50 W power. As a result of the procedure, the ITO layer of 100 nm thickness was created with a high reproducibility factor.

SiO_2 deposition

The inductively coupled plasma enhanced chemical vapour deposition (ICPECVD) method, known for the production of highly uniform silicon dioxide films, allowed us to deposit SiO_2 on the Si/ITO wafer. It was done with Oxford PlasmaPro 100 ICPECVD module. The process was performed in 150°C and took exactly 30s. During deposition, the pressure in the chamber was kept at 2.5 mTorr with a fixed ICP power of 2500 W. Flow rates of 0_2 and SiH_4 gases were set to 32 sccm and 26 sccm, respectively. Due to the very quick procedure, the thickness of the layer deviated between 57 and 61 nm.

OTS silanization

Octadecyltrichlorosilane (OTS) binds with SiO_2 and forms a self-assembled monolayer on top of it drastically changing the water affinity of the SiO_2 surface [29, 34]. Multiple Si/ITO/SiO_2 12x12 mm pieces were arranged around a PTFE round dish placed in a homebuilt vapour coater system connected to a SalvisLab Vacucenter VC 20 vacuum oven. The oven was then heated up to 125°C. In the meantime, 200 µl of OTS was measured with the pipette and carefully transferred to a Teflon dish in the oven. From that moment on, the oven doors were kept closed and sealed under a 10^{-2} mbar vacuum. The samples were left in the oven for 1 h from the moment when the operating temperature had been reached. Prior to the removal of the samples, the oven was flushed with nitrogen a couple of times to eliminate toxic gases that might have been formed during the procedure.

Conctact Angle Measurements

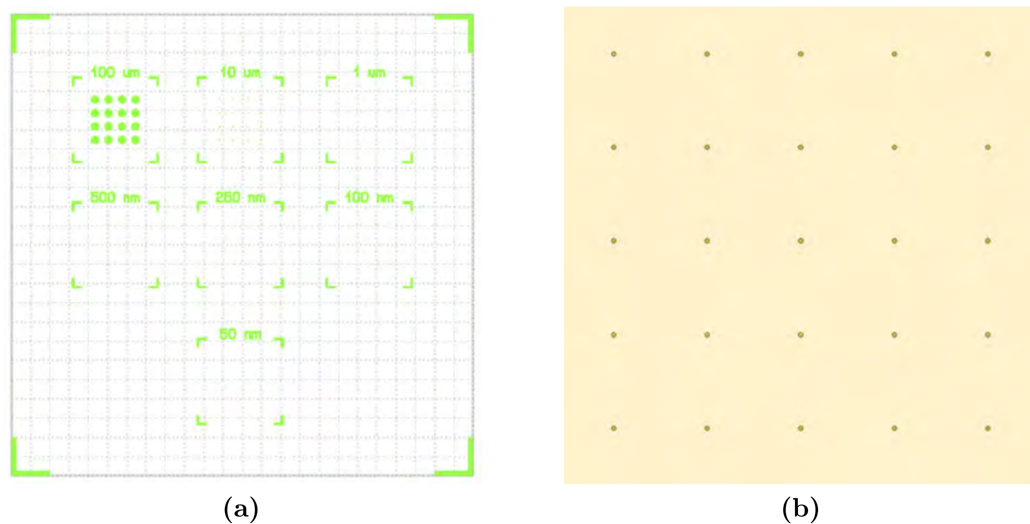
The contact angle measurements were performed on the Ossila Contact Angle Goniometer with a monochromatic light source and a high-resolution camera to record the videos further interpreted on the PC software. By comparison of droplet models to the images captured by the system, the degree of surface wetting was indicated.

Spin-coating the resist

Süss MicroTec Delta 80 Spin coater was utilized to coat the sample with a resist. Working procedures such as rotating speed, length of the process, and baking time were adjusted depending on the type of resist and desired thickness of the layer. For CSAR the spin-coating step took 45 s with a rotating speed set to 4000 rpm and 1000 rpm acceleration, followed by 3 mins of baking in 150°C. For S1813 the procedure took 40 s with identical parameters: 4000 rpm rotating speed and 1000 rpm acceleration. It was then baked for 1 min in 115°C. Received spin-coated layer thicknesses were between 75-80 nm for CSAR and roughly 1.5 µm for S1813.

Patterning the holes

Two available methods to pattern micro- and nanoscale structures available in AMOLF's cleanroom were tried to evaluate and compare the outcome.



(a) (b)

Figure 3.1: Desings of the micro- and nanostructures patterned on each 12x12 mm sample. **(a)** E-beam lithography design. **(b)** UV lithography design.

E-beam lithography was carried out on Raith E-line lithography system (Voyager) using dual beam exposure to pattern >1 µm features, such as markers and bigger holes, with a high current beam (HCB) to save some time and smaller objects with a low current beam (LCB) to guarantee the optimal patterning resolution. The calculated beam current used in HCB amounted to 4.0473 nA, with an area dose of 200 µC/cm^2 and 50 nm step size. For the LCB the beam current equaled 0.12841 nA, with an area dose of 130 µC/cm^2 and 5 nm step size. At the end of the procedure, structures were developed by placing a wafer in n-amyl acetate for 1 min, followed by 8 s in o-xylene, 15 s in MIBK 9:1 IPA, and rinsing off with IPA.

UV-Mask lithography was performed on Suss MABA6 UV Mask aligner with SCIL. The machine was operated in hard contact mode, sticking the sample firmly to the mask (Mask 046 from the cleanroom). The exposure time was set to 8 s with a 25 mJ/cm^2·s power giving 200 mJ/cm^2 in total over the whole duration of the procedure. To develop patterned structures each piece was dipped in MF-319 developer for 1 min and stirred vigorously, then moved to the beaker with H_2O to dilute the toxic TMAH.

Patterning designs

The initial idea with e-beam lithography was to investigate how the size of the device will influence its properties, so we aimed to pattern 7 regions with holes of different sizes on a single piece. Each region consisted of a 4x4 array of holes in a square distribution. The hole diameters were varied and amounted to 100, 50, 10, 1, 0.5, 0.25, 0.05 µm which is shown in Fig. 3.1a. The position of the centres of the holes was kept constant so they were not impacted by a change in hole diameter. Big markers were added to indicate the line along which the samples should be diced and make it easier to find a specific region on a sample. For UV mask lithography we used a mask with a large array of holes of the same 5 µm diameter and 150 µm spacing between them (Fig. 3.1b). A separate subsection is focused on the outcome of patterning.

Etching through SiO_2 layer

To etch through the silicon dioxide film, the Oxford Plasmalab 80+ was used. We took advantage of a standard program SiO_2 basic utilizing 300 W of forward power in the presence of 2 gases in the chamber, namely 0_2 and CHF_3. The pressure inside the chamber was set to 30 mbar. The plasma etching was performed for 100 s with a DC bias voltage circulating around 480 V throughout the procedure.

Resist Removal

The acetone bath is usually enough to remove the resist after the lithography process but after plasma etching more violent measures were needed. The procedure relied on transferring the pieces to the beaker filled with acetone straight after taking them out from Plasma 80+ and placing the beaker into the Branson 2800 ultrasonic cleaner, which uses 40 kHz frequency, for 10 min on its maximal power. One should keep an eye on the beaker for the entire duration of the sonication because there is a risk of acetone starting to burn due to excessive energy.

Filling the holes

The perovskite work was performed in the glovebox with an N_2 atmosphere, O_2 level below 1 ppm, and H_2O level below 0.5 ppm. The chemical scale and pipettes were used to measure desired quantities of chemicals in solid and

liquid form, respectively. A certain amount of MAI and PbI_2 powders was first calculated to get the solutions of exactly the same molar concentration. They were then weighed on a scale and placed in a vial. The vials with stirring bars in them were filled with a certain amount of dimethylformamide (DMF) and placed on the magnetic plate to activate the stirring and ensure that the material will be fully dissolved. The MAI + DMF solution was transparent while PbI_2 + DMF was yellowish in colour. The concentrations of the substrate solutions created in this work were 0.02 M, 0.2 M and 1 M. For instance, to make a 0.2 M solution of MAI + DMF 0.0318 g of MAI was mixed with 1 ml of DMF, whereas to make a 0.2 M solution of PbI_2 + DMF 0.0922 g of PbI_2 was mixed with 1 ml of DMF.

Once both MAI + DMF and PbI_2 + DMF solutions of the same concentration were ready, they had been transferred into a new empty vial in the 1:1 volume ratio with a pipette. Hence, the MAPI precursor solutions of 0.01 M, 0.1M and 0.5M that had a mild yellow tint were technically prepared. Before the experiment, we transferred each solution to a fresh vial with a syringe. Before pouring it to the vial we placed a PTFE 0.2 µm filter on a syringe to eliminate possible material aggregates. Such a precursor could be used for further experiments.

The procedure of filling the holes with the perovskite was conducted on the hot plate. At first, a silanized sample was placed on a hot plate preheated to 50°C, then either 20 µl or 50 µl of the filtered precursor was drop-casted on the sample. A flat PDMS sheet was mounted to the glass slide with its soft side, so the hard side could face the sample ensuring the best possible contact. A glass slide with a PDMS stamp and 3.2 kg heavy scale weight were then used to apply the external pressure on the sample.

Au evaporation

Top electrode was evaporated on the samples with the use of Polyteknik Flextura M508 through electron beam physical vapour deposition (EBPVD). Gold was the evaporated material and the selected heating mode was Au soak. The PC evaporation pressure during the procedure amounted to $9.31e^{-7}$. The desired evaporation rate of 0.05 nm/s was reached with an emission current of 42 mA. The procedure was stopped when the thickness of the gold layer reached 80 nm.

3.2.2 Characterization

Layer thickness measurements

The thicknesses of ITO and SiO_2 were measured with Thin Film Analyzer Filmetrics F20 UVX that fits the thickness of a given material to the measured light reflection of the surface with a 1 nm accuracy, whereas photoresist thicknesses were confirmed with the use of a KLA Tencor Stylus Profiler P_7 profilometer that is able to mechanically establish height differences with a sub-angstrom resolution.

Structural measurements

To investigate how different fabrication steps went and establish if perovskite ended up in the holes, an optical microscope operated in a bright field mode with a magnification range of 5x, 10x, 20x, and 50x was frequently used. Scanning electron microscopy (SEM) performed on FEI Verios 460 with a working distance of 4 mm, operated in 2 kV and 100 pA, was utilized to get more insight into the morphology of the perovskite crystals that grew in the holes.

Optical measurements

PL maps of the promising samples were measured to prove that MAPI was successfully deposited in the holes. It was done using a WITec microscope system with a built-in CCD spectrometer (Andor iDus DV401A BV). The measurements were conducted at room temperature with an operating power of 300 µW.

3.2.3 Electrical measurements

To study the electrical properties of the final device a probe station connected to an Agilent B2902A Precision/Source Measure Unit (SMU) was used. The single pixels were separated by manually scribing a square in the gold electrode around a perovskite-filled hole using a tip of a probe. The high-force tip was placed in contact with a perovskite inside the isolated gold square, whereas the low-force tip was put in contact with the ITO layer. The IV curves were measured by sweeping between -1.5 V and 1.5 V at a rate of 0.45 V/s.

Results and Discussion

In this section, a summary of the most significant results and key findings will be presented accompanied by a thorough explanation of observed features and complications. Upon reading this chapter, the reader should become familiar with the final architecture of the created device, understand how it was manufactured, and how the holes were filled with $MAPbI_3$. Both the potential and limitations of investigated perovskite incorporation methods will be addressed. The proof of successful growth of perovskite within 4-5 µm holes will be showcased by the results of structural and optical analyses. Ultimately, information about the electrical properties of the final device will be given.

4.1 Device Architecture

The final device is depicted in Fig. 4.1. A thin layer of oxygen-deficient ITO was chosen as a bottom electrode following its high conductivity and high number of charge carriers [33]. SiO_2 can be easily etched through and is proven to passivate the movement of ions and degradation of the material [35], hence it was used as a spacer layer in which the perovskite was grown. From the range of halide perovskites, $MAPbI_3$ was selected to be an active layer in our device since it exhibits mixed ionic-electronic conduction, has a very low activation energy of ion migration, and a tunable bandgap but also is easy to grow and considerably well-documented for the perovskite material [6, 10]. We have chosen OTS to manipulate the contact angle of the SiO_2 layer since it is one of the most common silanizing agents [34]. Both gold and silver are often used as a material for the top electrode. Since this research aimed to exploit the movement of iodide vacancies in the halide perovskite to see the hysteresis, gold was a better choice for the top electrode than silver because of the lower mobility of Au^+ ions [13].

Figure 4.1: Final device architecture. All of the materials are listed in the correct order and their thicknesses are provided. Self-assembled monolayer of OTS is depicted as a very thin blue line on top of the SiO_2 layer.

4.2 Fabrication overview

Device formation involved multiple steps and many fabrication techniques to perfectly recreate the outlined design, what is shown in Fig. 4.2.

Initial steps

The silicon wafer was stored in a dustproof box so it did not require any further processing. The ITO and SiO_2 were deposited according to the procedure described in the 3.2.1 subsection. Aside from the visual inspection of the deposited films after the processes, the layer thicknesses of 100 nm and 60 nm of ITO and SiO_2, respectively, were measured with the filmetrics thin film analyzer to confirm that everything went as planned.

4.2.1 OTS silanization and contact angle measurements

Two methods were investigated to find the best way to silanize our samples. The first one was inspired by Wang et al. work where they placed the wafer in a hexane 500:1 OTS solution and left it inside for 10 min, further rinsing it with acetone [29]. In our case, contact angle analysis indicated that the wafer was not silanized uniformly and the degree of increase in contact angle was much smaller than expected (see Appendix 8.1). The other experimental technique relied on placing the samples in a vacuum oven with liquid OTS,

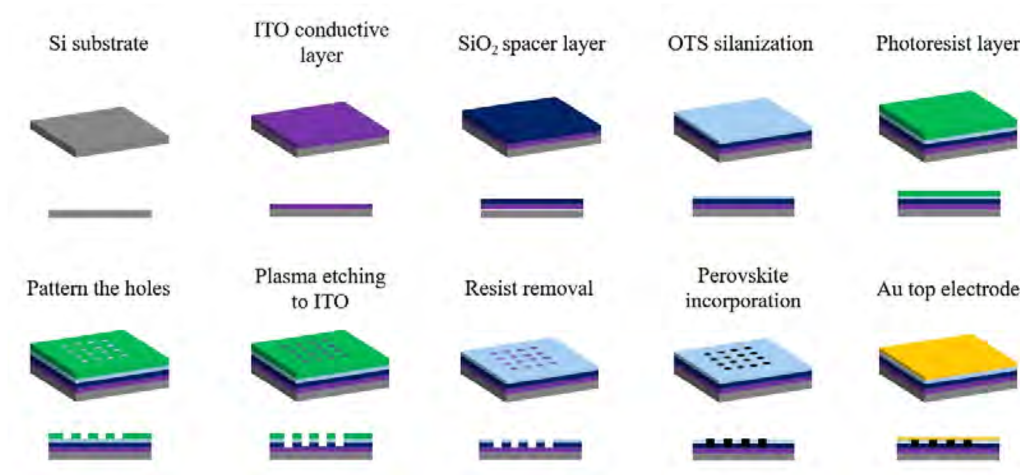
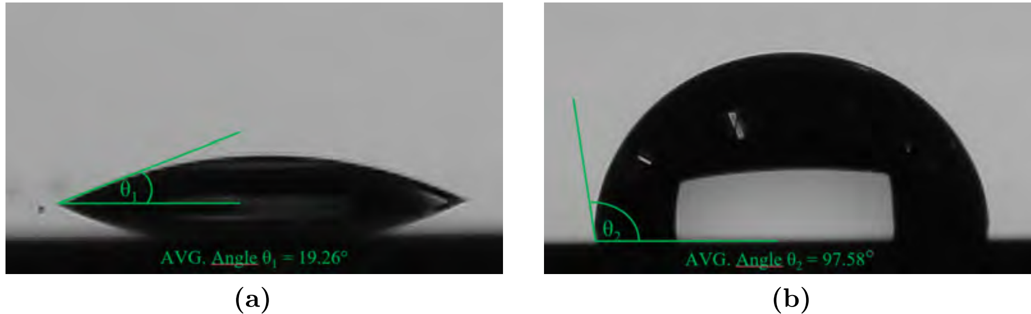


Figure 4.2: Detailed overview of the fabrication steps.

evaporating it, and coating the samples with vapour. The results of our attempts are depicted in Fig. 4.3. It is clearly visible that the contact angle before and after silanization changed dramatically, which is caused by the formation of a self-assembled monolayer of OTS on the SiO_2 surface. The significant difference in SiO_2 average contact angle of about 80°, leading to the final value of $\theta_2 = 97.58°$ let us assume that any liquid should favour the ITO surface, especially with an average contact angle of ITO being around 57° (see Appendix 8.2).

Spin-coating the resist

A major problem was encountered during the spin-coating of CSAR on the silanized pieces. Unlike the regular SiO_2 surface which was easily coated with such a resist, the silanized one was never coated. The resist was simply falling off the piece during spin-coating because of its hydrophobicity. Various attempts were made to go around this problem including silanizing after patterning or using PMMA instead of CSAR but non of these ended up being compatible with our approach to create the hydrophobic/hydrophilic regions on a sample's surface, therefore controlling where the perovskite grows on our sample. On the other hand, the spin-coating of S1813 was not affected at all by OTS silanization. Each spin-coating procedure was followed by the thickness analysis of the spin-coated photoresist. No matter the type



(a) (b)

Figure 4.3: Camera images of H_2O droplet spilled on SiO_2 surface with the results of respective contact angle measurements. **(a)** Before silanization. **(b)** After silanization.

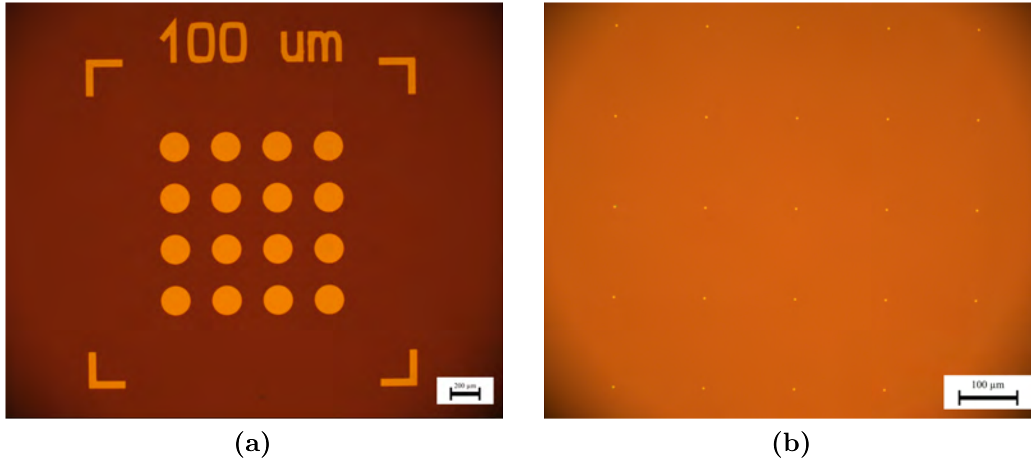
of resist, it was done on the profilometer. CSAR on not-silanized pieces had a reproducible thickness of 75 nm, whereas S1813 on both silanized and not-silanized pieces, had a thickness of 1.5 µm.

4.2.2 Holes patterning

In addition to the contact angle measurements, the holes patterning step brought us some pivotal results as well. Originally, e-beam lithography was the only method considered to pattern the micro- and nanostructures in this study. Due to a few setbacks with the Voyager apparatus, the decision was made to test the UV lithography too. Based on the fact that both patterning designs were successfully obtained (Fig. 4.4), we could distinguish differences between the two methods, list their advantages and disadvantages, and highlight why we have proceeded with the UV Mask technique after all.

E-beam lithography

E-beam lithography offers myriad possibilities in terms of patterning structures of any size and shape. Its substantial advantage comes from the fact that with proper software the patterning design can be adjusted to one's needs at any time. The sizes of the biggest and smallest holes from our design, 100 µm and 50 nm, respectively, corresponded to the operating limits of the device. In Fig. 4.4a a microscope image of the region with the largest features is presented. All of the holes were identical and their circular shape was



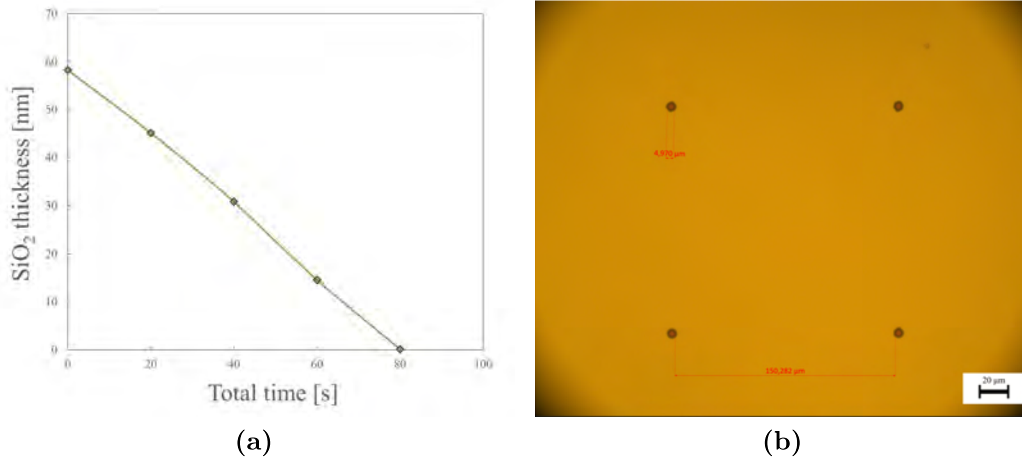
(a) (b)

Figure 4.4: Optical microscopy images of patterned structures. **(a)** Patterned E-beam lithography design (zoom-in to the region with 100 µm wide holes). **(b)** Patterned UV lithography design.

flawlessly preserved but their diameter was 2x the expected one. It must have come from a manual mistake while setting up the program in the Voyager. The patterning was done on a full wafer, so a lot of time was saved. However, as a consequence of very high degree of complexity of the design the procedure itself took roughly 40 hours. Once the procedure has finished, one had a wafer with 40 pieces ready to be diced and used for further experiments. Unfortunately, we could only pattern the design on non-silanized surfaces which stopped us from proceeding with this method.

UV-Mask lithography

UV Mask lithography offers similar prospects as e-beam one but works on a different basis. The parts of the resist that are exposed to UV light are hardened and cannot be washed off after the procedure. The mask with a certain pattern is used to block the incoming light and allow for patterning. In our case, it was a mask with multiple patterning designs, from which we have chosen the one with a square array of 5 µm holes separated from each other by a constant value of 150 µm, which is depicted in Fig. 4.4b. The size of the holes remained uniform but their shape was not as perfect as in the instance of e-beam lithography. The masks are being cleaned after every use



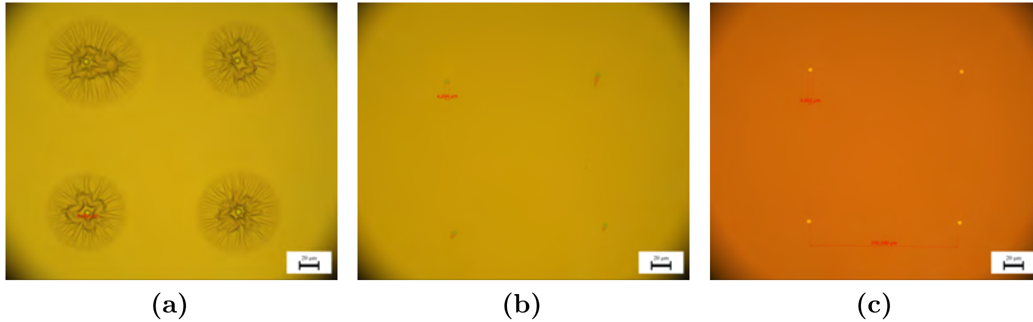
(a) **(b)**

Figure 4.5: Characteristics of etching procedure. **(a)** Plot of SiO_2 thickness vs time of etching. **(b)** OM image of holes after the etching procedure.

but naturally, the features are still going to degrade over time which may be a source of the resolution loss. The mask that we had allowed us to pattern only a single piece at a time but the procedure time was extremely quick - about 8 s. The crucial benefit of the method was the ability to pattern structures on silanized surfaces. It is worth mentioning that there is an option to order a mask with a more complex, desired design although the expected waiting time forced us to stick with the available one.

Etching through SiO_2 layer

For the perovskite to reach the ITO layer we had to etch through 60 nm of SiO_2 leaving none of it in the hole area, using the procedure listed in 3.2.1 subsection. Several tests were performed to adjust the etching rate with and without photoresist on our sample (Fig. 4.5a). After each step, the thickness of the SiO_2 layer was measured with a filmetrics thin film analyzer. Eventually, we established the average etching rate to be 0.75 nm/s so 80 s was enough to etch through the entire layer. Since the rate was moderately different for each etching step we added additional 20 s to the procedure to make sure that SiO_2 is completely gone from the holes. The shape of the holes was more irregular after the procedure and their size deviated slightly from the starting point but still circulated around 5 µm (Fig. 4.5b).



(a) (b) (c)

Figure 4.6: OM images of the array of 4 holes after different resist removal approaches. **(a)** 2 h of regular acetone bath. **(b)** 3 h of acetone bath heated to 45°C. **(c)** Acetone bath immediately subjected to 10 mins of high power sonic treatment. Red markers indicate the diameter of the holes.

Resist Removal

It is very important to remove the polymer resist from the sample as thoroughly as possible as the results pinpointed the tendency of perovskite to grow on the resist residues. It is going to be explained in the 4.3.2 subsection. Such leftovers were mainly found in the form of tails around holes, which was a consequence of drastically reduced solubility of the resist in the developer after UV exposure. The acetone bath was clearly not enough to remove the resist from around the holes (Fig. 4.6a). The addition of heating helped but not to a satisfying degree (Fig. 4.6b). Finally, by combining the acetone bath with a 10 min high power sonication, we were able to remove resist from our sample almost entirely (Fig. 4.6c). It is crucial to indicate that the sonication should be performed straight after etching to ensure the efficiency of the resist removal. All of the images depicted in Fig. 4.6 highlight that in spite of the resist removal technique, the size of the holes was always considerably smaller (around 1 µm) after this procedure.

4.3 Perovskite Incorporation

The second major part of the project constituted all the work with perovskite, starting from confining its growth to the patterned holes, followed by characterizing its quality and investigating the properties of the final device.

4.3.1 Precursor preparation

To utilize our technique based on the difference in contact angle between the ITO and SiO_2 surface, we had to acquire the perovskite precursor solution first. To do that we have followed the procedure listed in the 3.2.1 subsection.

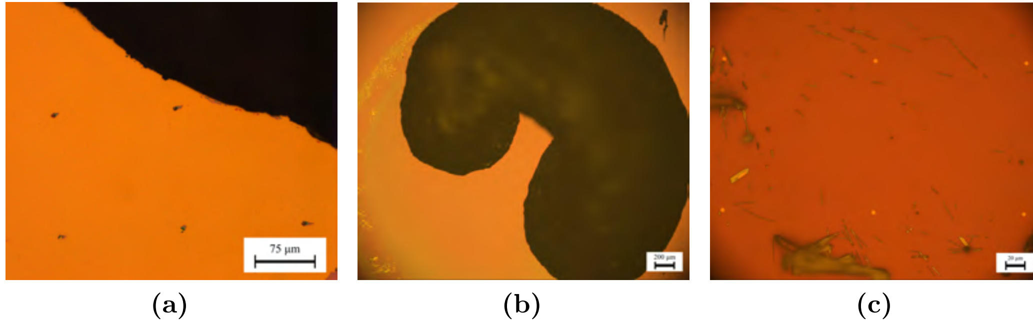
4.3.2 Tested methodology

All of the tested perovskite incorporation methods relied on evaporating the DMF from the precursor solution and exploiting the decreasing solubility of $MAPbI_3$ in the solvent when the temperature rises above 60°C [36].

Drop-casting

We started off with the simplest method which consisted of drop-casting the perovskite on the sample placed on the hot plate and growing the perovskite by manipulating the temperature. Both 20 µl and 50 µl of 0.01M and 0.1M precursor solution was drop-casted on a single silanized piece preheated to 50°C. Altogether there were 4 pieces for a single experiment kept at 50°C for 1 h. Afterwards, the temperature was increased to 70°C. In 15 mins the solvent was completely evaporated, hence samples were removed from the hot plate.

The summary of the experiments is depicted in Fig. 4.7. Fig. 4.7a refers to the results of the very first experiment where we observed a perovskite in the holes. Upon further magnification, we saw that the perovskite is likely to grow on the photoresist leftover tails around the holes rather than in the holes themselves. Fig 4.7b illustrates how MAPI actually crystallized on top of our sample. Since the precursor solution did not wet the surface and stayed on it as a droplet, the perovskite grew up in the form of a "mountain". This behaviour is a direct result of a coffee stain effect [37]. We still hoped that the holes underneath the mountain might be filled with perovskite so we removed



(a) (b) (c)

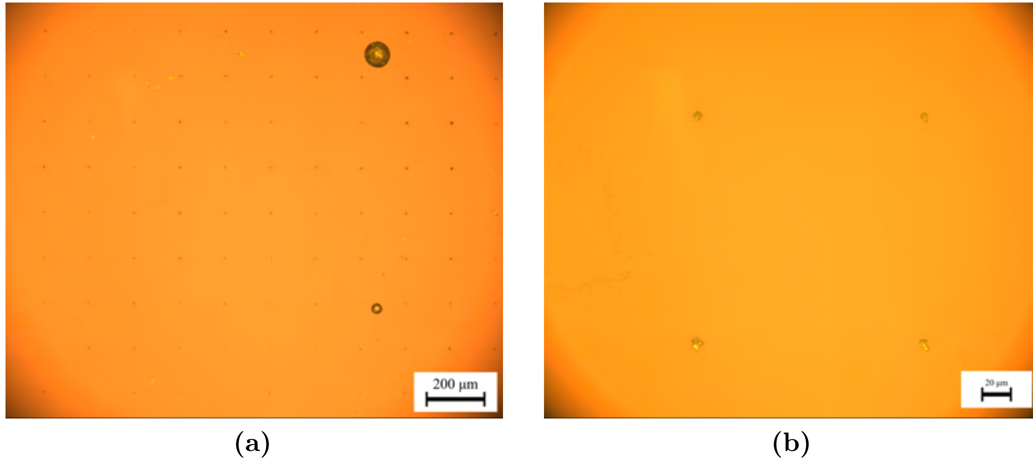
Figure 4.7: OM images condensing the results of the drop-casting method. **(a)** Holes with perovskite growing on resist leftovers. **(b)** Perovskite mountain which grew on top of the sample. **(c)** Empty holes discovered after removal of perovskite mountain.

it mechanically. Alas, the holes were empty after the removal, as can be seen in Fig. 4.7c. The simplicity of the method resulted in a very low prospect of successful perovskite incorporation into the holes. At last, we found out how important it is to clean the samples from any resist leftovers.

Combination of drop-casting and stamping

Given the expertise gained by numerous tests of a drop-casting method, we have committed to perfecting the method by applying external pressure to the system, therefore actively forcing the $MAPbI_3$ precursor solution to end up in the holes.

The approach was very similar to the previous one but additional steps of placing the glass slide with PDMS stamp and the scale weight on the sample were added. In this case, we drop-casted either 20 µl or 50 µl of precursor on top of the sample preheated to 50°C. The concentrations of the precursor used in this method were 0.1 M or 0.5 M. Straight after the solution was drop-casted on the sample's surface, we placed a glass slide with a PDMS stamp on a sample aiming for the centre of the droplet and followed it with a scale weight. The heating process had to be extended and the temperature had to be increased as it was much harder for the liquid to evaporate from underneath a stamp. After a series of experiments, the heating procedure was established. It consisted of 1 h at 50°C, 45 mins at 80°C, 15 mins at



(a) (b)

Figure 4.8: OM images condensing the results of the combined drop-casting and stamping method. **(a)** The square array of 99 holes filled with $MAPbI_3$ **(b)** Zoom-in into the 4 holes filled with $MAPbI_3$.

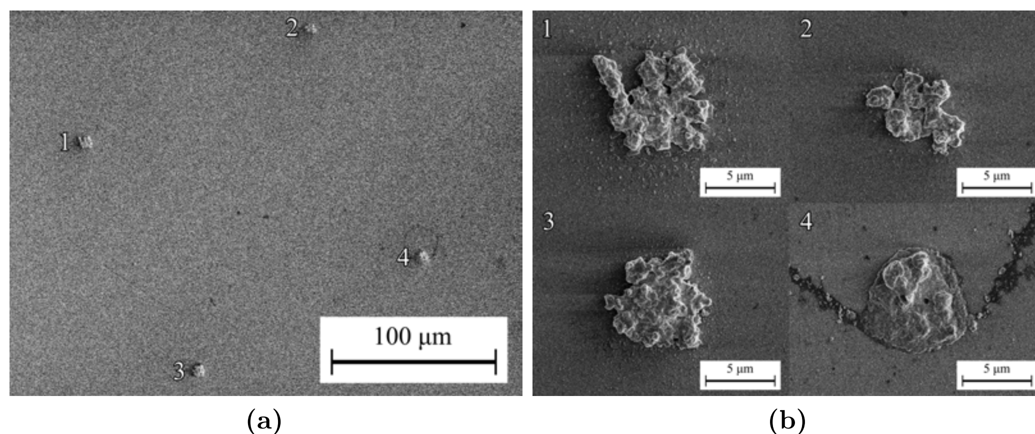
100 °C, removing the weight and stamp and leaving the sample for another 5 mins at 100 °C without the external pressure to evaporate the leftover solvent. A result of this technique, that is, a sample with successfully filled holes, is showcased in Fig. 4.8. The silanized surface looked almost empty, some bigger perovskite aggregates were notable but what is most important the vast majority of the holes seemed to be filled with the perovskite. In order to prove that we had to perform additional investigation.

4.3.3 Structural properties

Apart from all of the optical microscope images made after each step of fabrication and perovskite incorporation, scanning electron microscopy was used to check that it is actually MAPI filling the holes and if any pinholes were present that could lead to short circuits after depositing the top electrode.

SEM

Fig. 4.9a provides the SEM image of a square array of 4 holes, demonstrating that the perovskite overflowed the holes. To get even more insight into the morphology of MAPI crystals, the zoomed-in image of each particular hole



(a) (b)

Figure 4.9: SEM images of holes filled with MAPI. **a)** The array of 4 holes. **b)** Zoom-in to each particular hole. The numbers indicate which zoom-in image corresponds to each hole in the less magnified image.

from the array is provided as well (Fig. 4.9b). It clearly shows that the MAPI crystals did not follow the circular shape of the holes, their surface is rather rough and the degree of overflowing is high as the irregular crystals are between 6 and 7 µm wide. The latter might arise from the leftover solution that remains on the sample after peeling off the stamp. Essentially, we would like to have perfect control over the morphology of growing MAPI crystals and there is a lot of room for improvement. Nevertheless, the situation displayed in Fig. 4.9b, where MAPI is overflowing the holes is better in terms of functionality than one in which there would be pinholes as it could lead to short-circuiting in the final device.

4.3.4 Optical properties

The analysis of optical properties of the contents of the holes allowed us to verify ultimately if it is actually MAPI within the holes. Through the analysis of the position, intensity and wavelength of the luminescence signal one can verify the location and type of the emitting material.

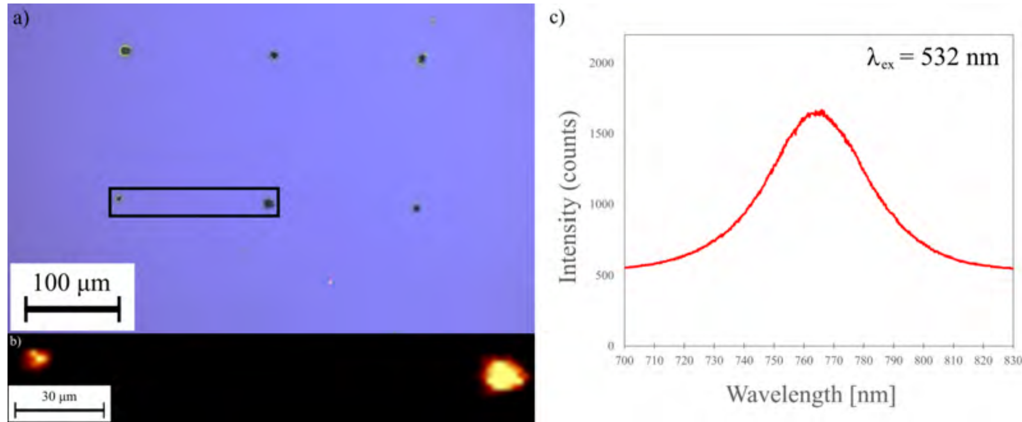


Figure 4.10: Summary of optical investigation of the sample filled with $MAPbI_3$. **a)** OM image of the array of holes. **b)** PL map of the region highlighted in subfigure **4.10a**. **c)** Luminescence spectrum of MAPI in the holes.

PL map

Photoluminescence mapping is a key technique in assigning the optical response of the system to the location. We took advantage of it to establish if there is any luminescence coming from our sample and if so, whether it comes from the holes or it is randomly distributed. The results of the scanning over the region highlighted in Fig. 4.10a containing 2 holes are plotted in Fig. 4.10b. The intense signal was not only visible but also it reflected the shape and position of the perovskite filling the holes. No signal was detected anywhere else which proves the selective growth of MAPI in the holes.

Luminescence spectrum

The luminescence spectrum of the signal detected throughout the PL mapping scan is plotted in Fig. 4.10c. Upon the 532 nm excitation, one can distinguish a single, broad band on the emission spectrum, characteristic of a perovskite material. It peaks at 765 nm which corresponds to MAPI's luminescence and validates that it is indeed MAPI in the holes.

4.3.5 Potential and limitations

The combination of drop-casting and stamping techniques delivered promising results regarding perovskite incorporation. The simplicity of the method and amount of mechanical steps implies that there is a potential for automation of the procedure what provides the prospect of efficient big-scale manufacturing. It is also wise to try to use different solvents like DMSO or DMSO mixed with DMF as it was proved that solvents have a crucial influence on the morphology of perovskite crystals [38].

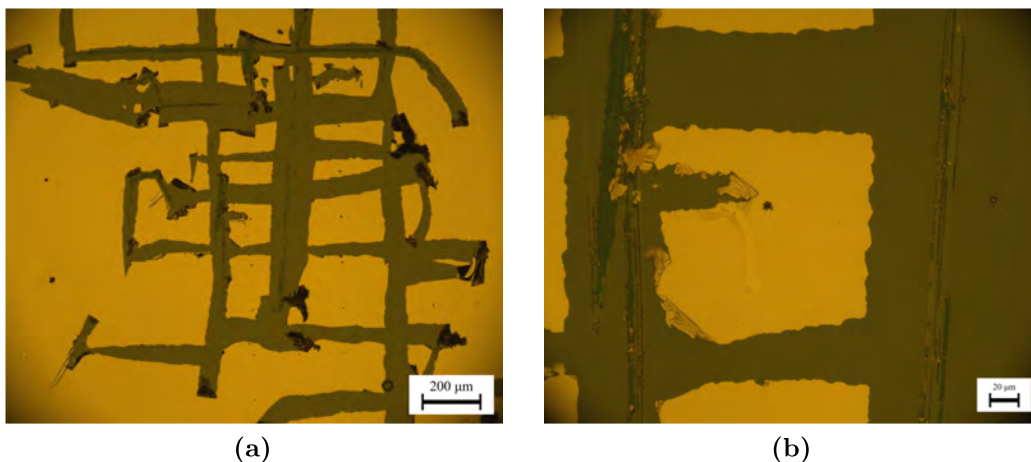
Nonetheless, the method requires a lot of improvements. Firstly, one would need to eliminate the issue of low reproducibility. Due to the manual placement of stamp and weight on the sample, the chance of smearing the precursor on the sample or spilling it off completely is high (see Appendix 8.3). It could be resolved by designing a device that would always place the external pressure in the same spot and with the same pressure. Another problem arises from stamp removal. Some material losses are expected during the lift-off of the glass slide with the PDMS sheet as the leftover solution makes it stick to the surface of the sample. Additionally, it limits the control over the morphology of perovskite crystals, especially if there is still some precursor solution left on the sample.

4.4 Device Characterization

On account of the successful fabrication of the device with perovskite in holes, its electronic properties could be examined. In the end, only the electrical properties of the final device were measured but these were crucial to signify the device's ability to be turned into an artificial synapse.

4.4.1 Electrical properties

The goal of the project was to make an artificial synapse. Through the analysis of the electrical properties of our device, we could establish if it truly acts as a memristor.



(a) (b)

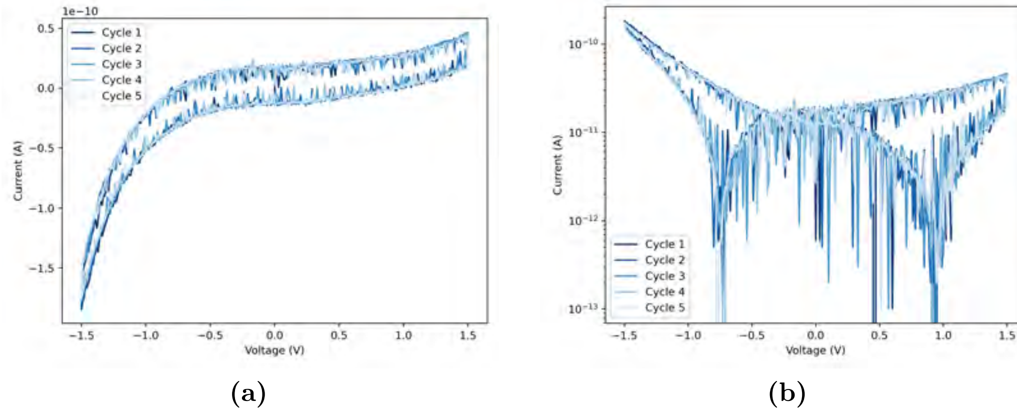
Figure 4.11: OM images of the sample with manually scribed gold squares. **(a)** Zoom in to the array of holes of showcasing the inaccuracy of the method. **(b)** Zoom in to a single hole with a notable scratch representing where the high-force tip was contacted.

Au evaporation

The last step of the fabrication involved the formation of a top electrode. Similarly to the initial steps, we had an established procedure that allowed us to evaporate 80 nm of gold on top of the sample without damaging the perovskite and other layers underneath.

Electrode separation

To perform the electrical measurements we needed to separate a single hole with perovskite from the rest. To do that we manually scribed the Au top electrode with a probe tip aiming to confine a hole with MAPI to a gold square. The results of the procedure can be seen in Fig. 4.11. Clearly, the method was very inaccurate but we managed to isolate several single pixels. Before the measurement, the low-force probe tip was in direct contact with the exposed ITO layer, whereas the high-force probe tip was in contact with a gold square, as close to the perovskite as possible (Fig. 4.11b).



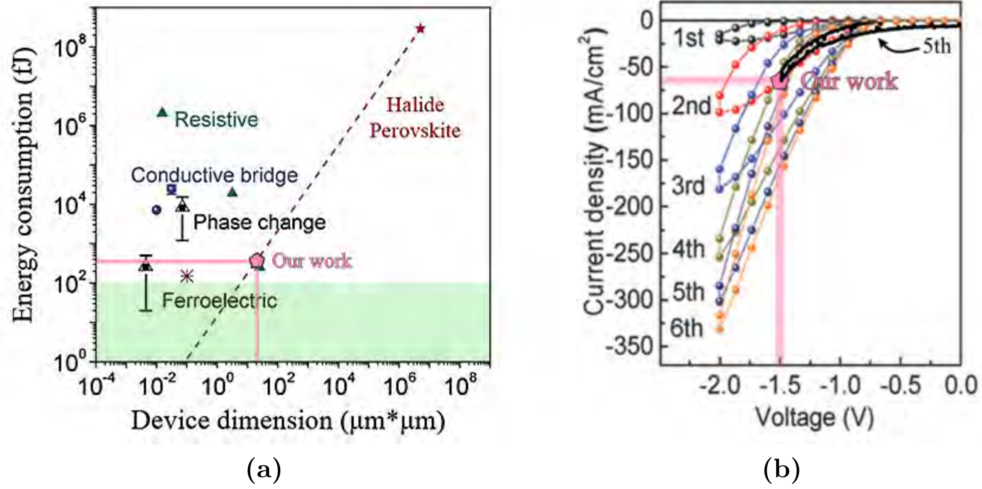
(a) **(b)**

Figure 4.12: The I-V curve of our device. **(a)** Plotted in a linear scale. **(b)** Plotted in a logarithmic scale.

I-V curve

The analysis of the relation between the applied voltage and the value of the readout current in the device is the easiest way to understand its electrical properties.

The I-V Curve of our device, which is a result of 5 voltage sweeps across the -1.5 V and 1.5 V range with the sweeping rate of 0.45 V/s, is presented in Fig. 4.12 both in a linear and logarithmic scale. The overall shape of the curve does not exactly match the desired hysteresis loop, distinctive for memristors. Upon reaching -1 V a drop in current is observed but it is not replicated in the case of positive voltage. The current offset throughout the forward and backward scan is presumably coming from the capacitance of the measurement setup, which is often an issue at such a low current regime. It should be possible to eliminate it by slowing down the scanning rate but due to the limited time, priority was placed on obtaining any results. Lastly, there was no current response when ITO and Au without perovskite were put in contact (see Appendix 8.4) so the signal plotted in Fig. 4.12 must have come from $MAPbI_3$ within the holes.



(a) (b)

Figure 4.13: Graphical comparison of our results to Xiao and Huang's calculations. **(a)** Theoretical magnitude of energy consumption for our device. **(b)** Plot of current density [mA/cm^2] vs voltage [V] of the 5th cycle of our device (black curve) overlayed with analogical results obtained by Xiao and Huang. Images reproduced from [3].

Some promising aspects could still be extracted from this data. Firstly, the current values are extremely low which was a key assumption in making an energy-efficient device. Therefore, it was extremely interesting to compare our results to the relations between the current and the size of the device calculated by Xiao and Huang [3]. We have to start by calculating the effective area of our device using the area of a circle formula 4.1

$$A = \pi r^2, \tag{4.1}$$

As was established in the subsection 4.2.2 the holes in which the perovskite crystals were deposited had a final diameter of around 4 μm. This gives us the value of r = 2 μm. In this case, the area of our device would be equal to 12.57 μm^2. Thanks to the structural investigation from subsection 4.3.3 we know that the perovskite crystals were actually irregular in shape and had a diameter ranging between 6 and 7 μm. To simplify the situation let us assume that they are actually circular with a diameter of 6 μm. This situation yields an area of 28.27 μm^2.

Looking at Fig. 4.13a we should then already be in the order of energy consumption of hundreds of femtoJoules per single synaptic event. At the same time, we know that the measured current values are on the order of $1e^{-7}$ mA. Hence, we can calculate the current density of our device. During the 5th measurement cycle, the current density of our device reaches its minimum of -62.257 mA/cm^2 at -1.5 V (eq. 4.2).

$$\frac{1.759e^{-5}\ [mA]}{2.827e^{-7}\ [cm^2]} = 62.257\ [mA/cm^2] \tag{4.2}$$

In this case, our results coincide with those obtained by Xiao and Huang (Fig. 4.13b) which confirms the potential of the device. Judging by the quality of the manually isolated holes (Fig. 4.11a) and manually placed contacts it seems obvious that there still is a huge room for improvement in these steps that should result in a better output.

Finally, it should be noted that there are a few ways that should help to get the desired hysteresis. Yan et al. indicated how important the proper selection of the electrodes is on the electrical behaviour of the final device [39]. Judging by the results obtained in their work it is seemingly worth investigating if swapping the top electrode material from gold to silver would induce the hysteretic behaviour. Besides, the grain sizes and overall crystallinity of $MAPbI_3$ considerably influence the extent of ion migration in the material [40]. Therefore, one could engineer the degree of hysteresis by getting more control over the growth of MAPI crystals in the holes and through modelling.

Conclusions and Outlook

Conclusions

The artificial synapse with a final structure of Si/ITO/SiO_2/OTS/$MAPbI_3$/Au was created in this work. Each step of the fabrication procedure of the device was well-documented. OTS silanization was performed with the vacuum oven as the samples made with the solution method were not silanized uniformly. An issue with a positive resist falling off the silanized sample prevented us from patterning with e-beam lithography. UV mask lithography was used to pattern the microstructures instead. To get the best out of the perovskite incorporation it is crucial to clean the sample perfectly from any resist leftovers, as perovskite tends to grow on them.

The combination of the silanized SiO_2 surface with the applied external pressure allowed us to confine the growth of perovskite into 5 µm holes patterned with UV lithography. The control over the morphology of the crystals was limited as they overflew the holes.

The IV curve of the final device did not show the hysteresis but the very low current values indicate that with a slight optimization of the procedure, it might arrive in the anticipated energy consumption regime.

Outlook

The are several notable ways to improve the fabrication, perovskite incorporation and characterization methods. In terms of the former, a different architecture should be considered that would limit the number of steps, therefore decreasing the overall costs of the procedure. Besides, one could definitely profit from finding the resist used in e-beam lithography that would stick to the silanized surface or design the architecture in which the silanization step could be omitted.

The key issue to resolve considering the drop-casting + stamping method is its reproducibility. A more automized setup in which the pressure would be always applied in the same spot on the sample and with the same strength would definitely be of great help. Moreover, a technique to place the PDMS

sheet on the microscope slide without any air bubbles could lower the extent of perovskite overflowing the holes.

A new much more consistent method to draw the electrode is certainly needed. There is a possibility to use a laser to scribe the gold square around the holed filled with $MAPbI_3$ but the array of holes would need to be always located in the same spot on the sample. It could be achieved with e-beam lithography where the whole wafer is patterned with the nanometer resolution. It is also important to consider the capacitance of the measurements setup while measuring such low current responses.

The desired hysteresis in the artificial synapse can be achieved through a few approaches such as exchanging the electrode material or establishing the perovskite grain size that would boost the degree of ion migration.

Acknowledgements

This extensive report would not come into existence without the help of many wonderful people to whom I am deeply thankful.

First and foremost, I want to thank Bruno Ehrler who gave me a chance to conduct this internship at AMOLF. His expertise in the field, valuable feedback, constant support and understanding helped me to get the best out of my time here.

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I would like to thank everyone in the Hybrid Solar Cells group too. Being surrounded by such a nice group of people that are experts in their field gave me no other choice than to constantly progress myself. I will miss the general funny atmosphere, coffee and lunch breaks together, not to mention the group outings, and chess games with Roman. I am certain that you are going to keep pushing solar energy research to new limits.

I cannot forget about Andries Meijerink who agreed to supervise the internship from the university side and grade this report. I was more than pleased to see him during my final presentation and answer his very insightful questions.

Lastly, I would want to appreciate AMOLF as a community of scientists in which I have prospered. I have never been in a place so full of compassion and lack of judgment which really changed my perspective on how the workplace should be organized.

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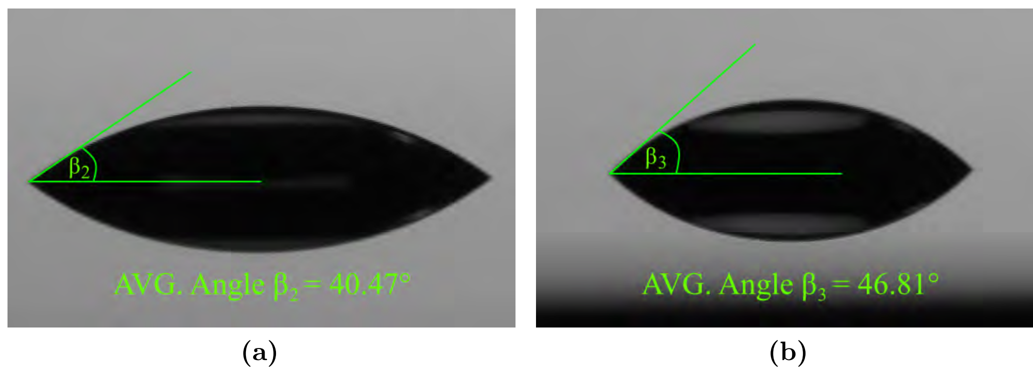
Appendix



(a) **(b)**

Figure 8.1: Camera images showing the unsuccessful silanization from solution. **(a)** Location 1. **(b)** Location 2. Because the wafer was much bigger than the platform of the contact angle goniometer, it looks like the droplets are floating in the air.

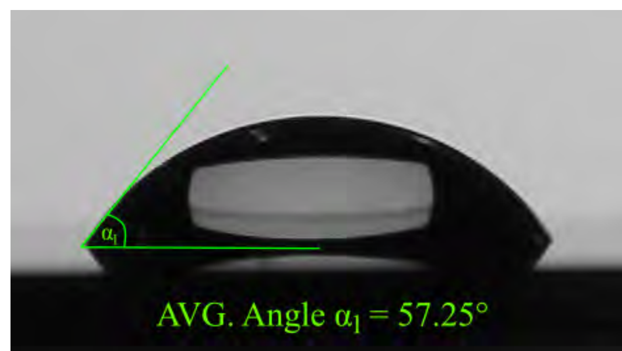
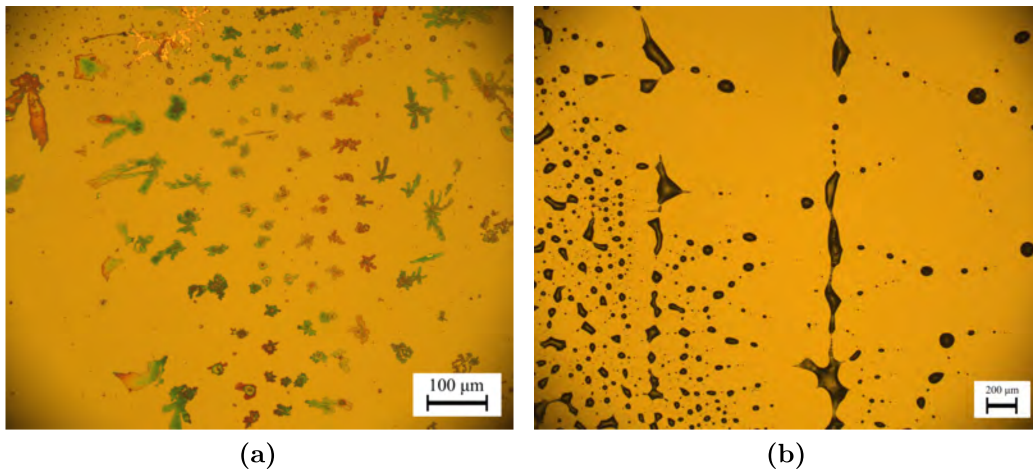


Figure 8.2: Contact angle measurements of not-silanized ITO layer.



(a) **(b)**

Figure 8.3: OM images with examples of what can go wrong while using the combination of drop-casting and stamping method. **(a)** Sample on which a lot of precursor solution was left and smeared over the sample. **(b)** Perovskite ended up growing randomly across the whole sample due to the displacement of the precursor while placing the stamp and weight.

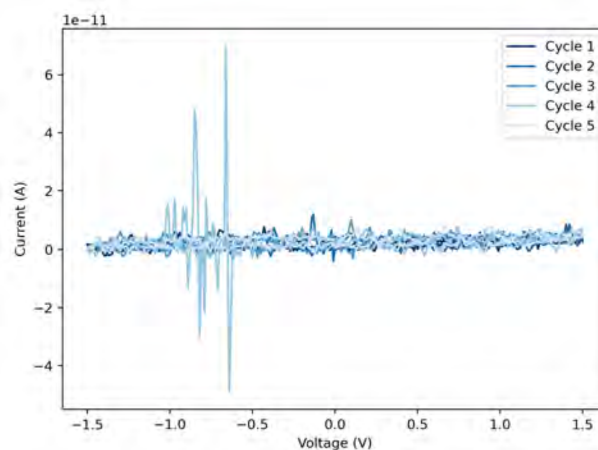


Figure 8.4: The reference I-V curve where contacts were made between Au and ITO but without the hole with $MAPbI_3$.