Fabrication and Electrical characterization of synaptic-transistor devices made of Hybrid metal halide perovskite

Master's Thesis by

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Abstract

The exponential growth of the capabilities of artificial intelligence (AI) models comes with a rise in computational demand and corresponding energy consumption, posing profound challenges to the long-term sustainability of the planet. Neuromorphic devices, designed to mimic the synaptic plasticity and neural dynamics of biological systems, present a compelling alternative.

A central component of neuromorphic hardware is the artificial synapse, with one notable approach to creating this component, being the utilization of a three-terminal synaptic-transistor device based on conventional field-effect transistor (FET) configuration. In these devices, the post-synaptic current can be modulated by a gate pulse, adjusting the conductance of the device, in a manner similar to the dynamic changes in synaptic strength observed in the brain.

This thesis investigates the utilization of $CH_3NH_3PbI_3$ hybrid metal halide perovskite material as the channel medium, leveraging its mixed ionic-electronic conductivity to emulate synaptic plasticity. Two different FET configurations are fabricated in a cleanroom environment. The channel dimensions are scaled down to micro- and nano-levels using electron beam lithography. Electrical characterization of the devices reveals their capability to emulate synaptic functions, through both electrical and light stimulation, highlighting the potential of halide perovskite artificial synapses for future low-energy neuromorphic applications.

Contents

Chapter 1

Introduction

1.1 The rise of Artificial Intelligence, energy challenges & neuromorphic hardware solutions

Artificial intelligence (AI) technology involves the capacity of machines to make decisions based on human behavior, employing processes such as perception, learning, and reasoning. The application of AI in multiple domains of everyday life proves to be invaluable and advantageous in saving time and enhancing work productivity, by automating the routine tasks previously handled by humans and performing them smartly and efficiently at accelerated rates, eliminating mistakes at the same time. For example, in the healthcare sector, AI assists medical teams in identifying, treating, and preventing diseases using evidence-based protocols and data-driven decisions [1]. In the field of customer service, AI chatbots provide quick, all-day-long responses to common inquiries, significantly reducing the need for human intervention and cutting response times [2], [3]. Additionally, in finance, AI-driven systems use machine learning to optimize investment strategies, customer engagement, and stock forecasting [4].

AI, also, contributes significantly to problem-solving and decision-making tasks as well as to innovation [5]. For example, AI customizes learning experiences and generates innovative educational materials using educational data [6]. In the medical field, AI helps in diagnosing diseases and provides healthcare services [7], [8]. Additionally, AI empowers businesses to develop effective marketing strategies and fosters innovation in the arts and cultural sectors [9]. Given its numerous advantages, AI technology is reasonably referred to as the driving force behind the 4th industrial revolution [10], bringing brilliant innovations across sectors like

healthcare, education, manufacturing, security, military, sports, agriculture, and transportation systems [5].

The significant impact of AI technology can also be understood if we consider how it is expected to affect the world's future economy. The global GDP is estimated to be 14% higher in 2030 because of AI [11]. The productivity improvements due to AI are expected to account for 50% of all GDP gains for the period between 2017 – 2030. As new technologies become more widespread and due to the increasing variety, personalization as well as improved quality of AI-enhanced products, consumer demand for those products grows steadily over time. As a result, 58% of global GDP in 2030 will come from those consumption-side factors (quality, personalization), as shown in **Figure 1.1** [11].

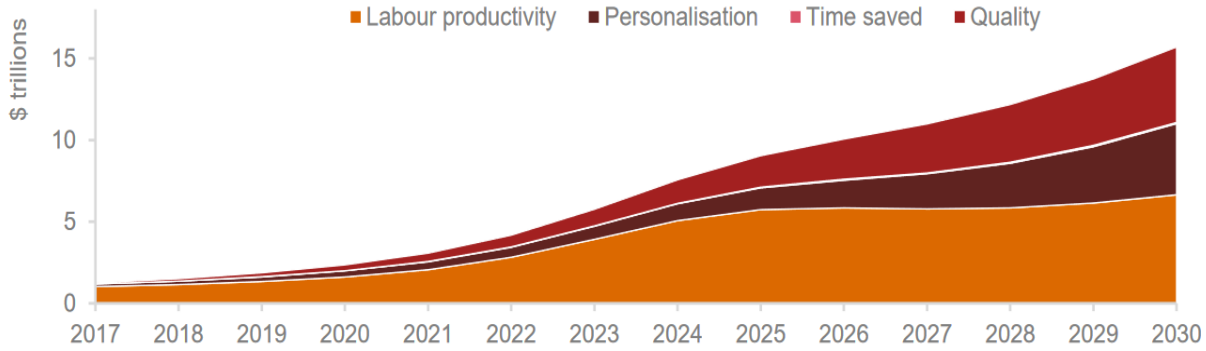

***Figure 1.1**: The global GDP impact by effect of AI 2017-2030. Figure taken from ref. [11].*

As AI technology rapidly advances and becomes more and more integrated into various sectors of people's lives, a significant concern arises regarding the growing energy footprint of Artificial Intelligence. AI algorithms are characterized by computational complexity and require a vast amount of data for training, while there is also the need for continuous learning and adaptation to new data [12]. As a result, the computational resources necessary to develop and maintain AI models and applications require massive amounts of energy. This is obvious, as shown in the **Figure 1.2**, where the energy consumption per request of the AI-generated ChatGPT platform and Google search engine, is calculated [13], resulting in three times higher energy consumption for the ChatGPT. This could cause a rise in data centers' contribution to global electricity consumption.

Moreover, according to Vries et al. [13], if Google integrated AI algorithms into its search engine, the power per request could increase 7 to 9 times higher, as shown in **Figure 1.2**, equating to the annual electricity consumption of a country like Ireland [13]. Those findings

indicate the crucial impact of AI technology on global energy consumption and the long-term sustainability of the planet. Advancements both in software and hardware technology are required to optimize the operation of AI algorithms and reduce energy consumption [13].

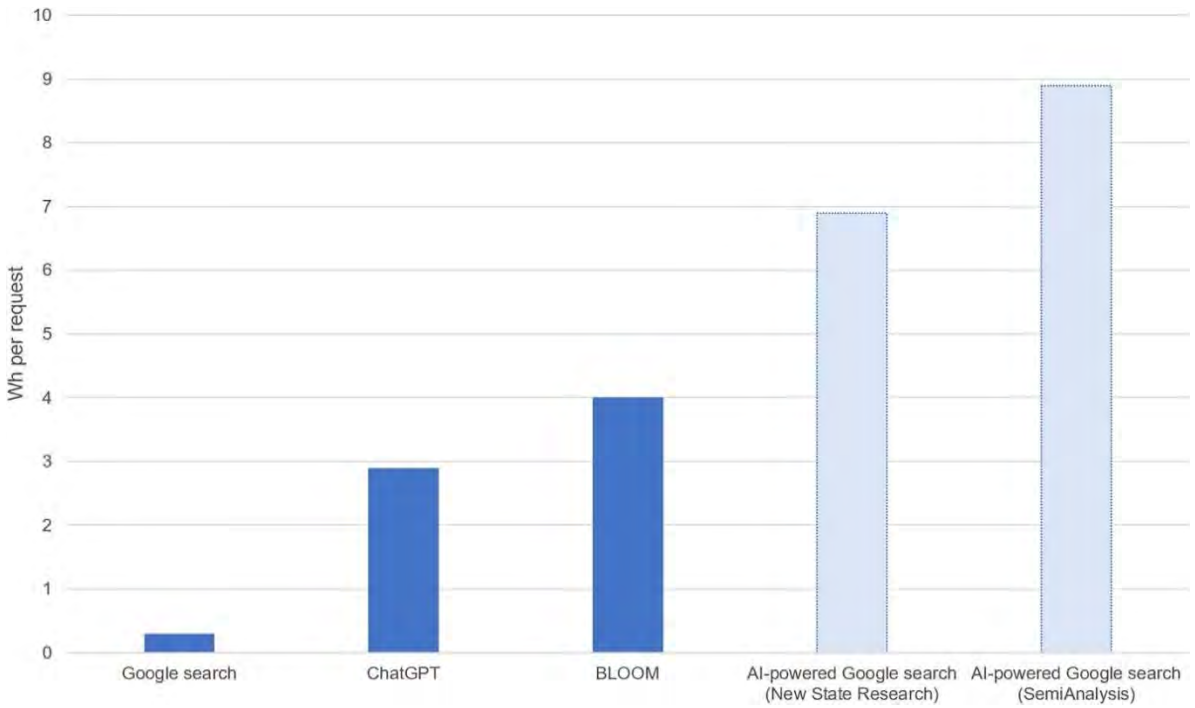

***Figure 1.2**: Estimated energy consumption per request for various AI-powered systems compared to a standard Google search. Figure taken from ref. [13]*

The main reason for the inefficient and energy-consuming running of AI algorithms is the current conventional computer technology, built on the Von Neumann architecture. In this architecture the processor and memory units are physically separated, thus the data must be transferred back and forth among those components. In the case of AI algorithms, the increasing amount of data transfer, between the memory and processing unit leads to high energy consumption and latency, limiting the system's capabilities [14]. To overcome this constraint, global research has oriented to different approaches inspired by biological concepts.

One of those approaches is the development of neuromorphic systems, namely computer architectures that mimic the way the information is processed in the human brain [14], [15]. In the human brain, the information is processed and stored simultaneously, so complex and parallel works are performed with approximately 10 – 20 W power consumption [16], [17], which is much lower than that of modern computing systems. For example, the energy consumption of a graphics processing unit (GPU), of typical desktop computers, that runs AI algorithms can reach up to 300 W [18]. If the contribution of other computer elements such as RAM, and CPU is also included, the energy consumption rises further, as reported by the

reference [18]. A comparison of the most significant computer functions between Von Neuman's computer architecture and Neuromorphic architecture is illustrated in Figure 1.3, while detailed information can be found in the reference [15].

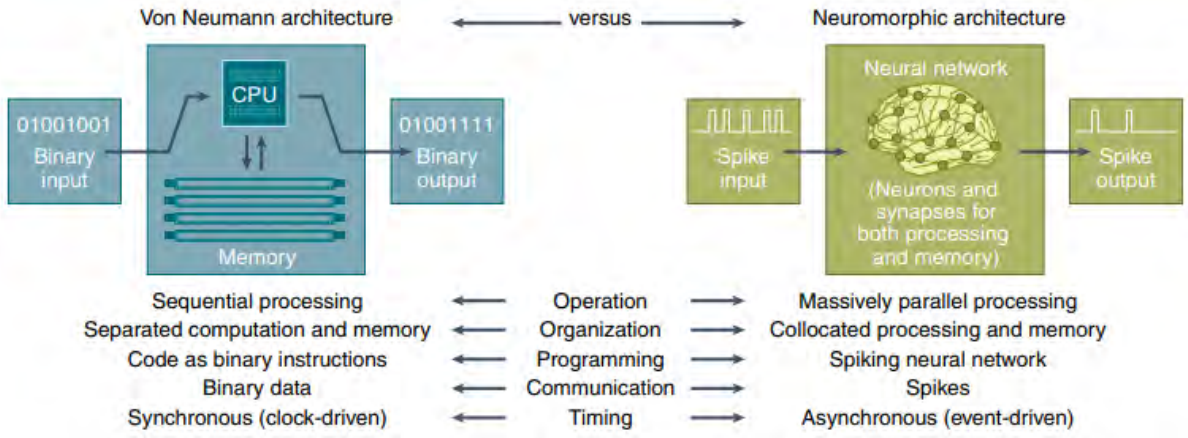

Figure 1.3: *Comparison of the von Neumann architecture with the neuromorphic architecture. The fundamental differences between the two architectures when it comes to operation, organization, programming, communication, and timing are depicted. Figure taken from ref. [15]*

Information is transferred by neurons, in the human brain. There are about 10^{11} neurons in the human brain and each neuron can have around 10^4 connections to each other to form 10^{15} synaptic nodes, which enables the brain to achieve an efficient information-transmitting system [16]. Neurons can strengthen or weaken their connection, demonstrating synaptic weight plasticity which is responsible for the most prominent learning and memory behaviors in the brain's cognitive system [17]. In reproducing the learning mechanisms of the human brain, neuromorphic computer architectures consist of numerous artificial synapses and artificial neurons. A remarkable example of neuromorphic hardware is IBM's TrueNorth chip with 10^6 neurons and $256x10^6$ artificial synapses, occupying a $4.3cm^2$ area [19]. TrueNorth's power density was calculated at 20 mW/cm^2, which is much lower compared to the typical power density of a central processing unit (CPU) of 50 to 100 W/cm^2 [19]. In general, the ideal candidate for replicating synaptic activities, in neuromorphic hardware, is a device capable of fully emulating the functionality of biological synapses.

Among emerging technologies, nanoscale memristive devices stand out as up-and-coming solutions for enabling synaptic activities in neuromorphic systems [17]. Memristive devices are two-terminal or three-terminal devices, in their simplest form consisting of two metal electrodes separated by a material, similar to a capacitor architecture. The resistance of the active material can vary depending on the bias voltage application between the two electrodes. The first electrode can be characterized as the pre-synaptic neuron while the other is the post-

synaptic neuron. This property enables the connection between the electrodes to strengthen or weaken, mimicking the synaptic weight plasticity of biological neurons, in the form of conductance changes.

The main objective of research in neuromorphic computing is to build memristive devices that can reach the ultra-low energy consumption of human biological synapses of 1-10 fJ per synaptic event (Kuzum et al. [20] provide an analytical explanation of how this value is calculated). Exploration of novel materials that can vary their conductance depending on applied bias will be needed to advance this goal. The most promising materials that are currently investigated range from magnetic alloys, metal oxides, chalcogenides, and 2D van der Waals materials [14], [20]. Organic materials seem very promising where sub-femtojoule levels have already been reported, for example, an organic synaptic transistor has been reported with energy consumption as little as 0.29 fJ per synaptic event [21]. However, their instability due to heat, water, and oxygen, the lack of a well-defined working mechanism, such as the formation mechanism of organic synapses, and the lower carrier mobility properties compared to inorganic semiconductors are disadvantageous for applications [22]. The field of neuromorphic computing is actively seeking sustainable materials that offer in-memory computing capabilities with ultra-low energy consumption and high stability.

1.2 Hybrid organic-inorganic metal halide perovskites for low-energy synaptic applications

In recent years, hybrid organic-inorganic Metal Halide perovskites (OHPs) have been extensively studied for their exceptional optical and electronic properties, making them promising candidates for use in photovoltaic applications [23]. This research has led to a significant increase in photovoltaic efficiency and a deeper understanding of the physical and chemical properties of OHPs. Recently, there has been growing interest in utilizing OHPs in other photonic and electronic devices, such as light-emitting diodes, X-ray detectors, and energy-conversion devices. It is estimated that OHPs will become key materials for next-generation devices soon [24]. Another advantage of OHPs is that they can easily be produced by low-cost large-scale manufacturing processes, as it is based on low-temperature solution-based fabrication [25]. On the other side, OHPs are easily degraded by exposure to light, moisture, heat, and oxygen [26], [27]. Consequently, a significant portion of scientific research is focused on improving the stability of OHPs.

Due to the soft and ionic nature of their lattice structure, OHPs exhibit both electronic and ionic conductivity. Ion migration is a major factor that limits the high performance of OHP devices by introducing hysteresis in the current-voltage characteristics. The low activation energy of ions, charge trapping mechanisms in grain boundaries, high defect density, and mixed ionic-electronic conduction all contribute to intrinsic hysteresis in the I-V characteristics of OHP devices [28].

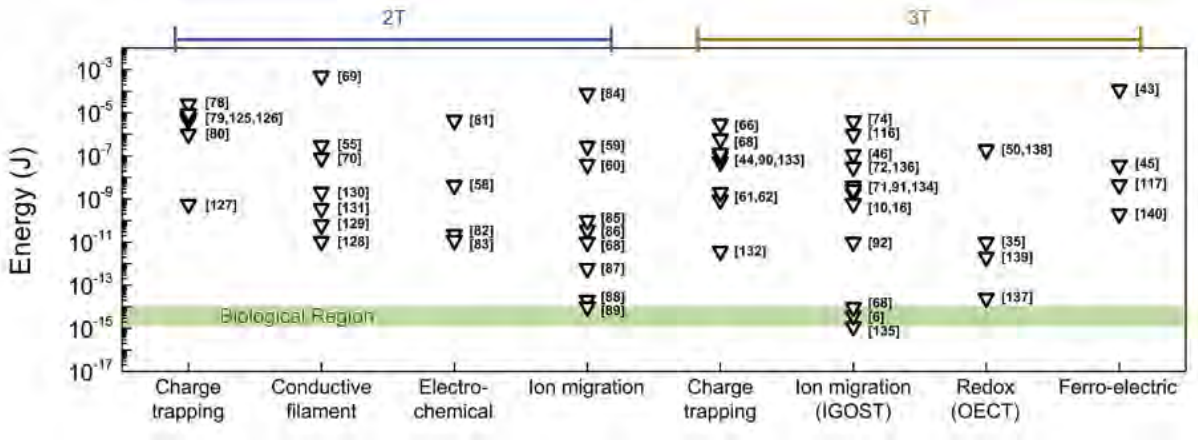

***Figure 1.4**: Energy consumption per synaptic event of organic artificial synapses depending on structures and working mechanisms. Figure taken from ref. [29]*

While this hysteresis is undesirable for most electronic and optoelectronic applications, it is beneficial for synaptic devices, as it enables access to multiple conductance states [30]. The low activation energy for ion migration indicates that only a minimum amount of energy per synaptic event is required for each operation, in synaptic devices, promising to reach the biological level.

In this work, the three-terminal synaptic transistor device is employed with the hybrid organic perovskite as the channel material using its ion migration mechanism for replicating synaptic plasticity. This type of device has the potential to approach energy consumption at the biological level as shown in **Figure 1.4** [29], where the energy consumption per synaptic event is plotted as a function of the working mechanisms for organic artificial synapses. One remarkable work of organic artificial synapses is the three-terminal electrolyte-gated vertical organic transistor of Liu et al. [31], where an energy consumption of 0.06 fJ per synaptic event has been achieved, significantly lower by biological synapses (1-10 fJ per synaptic event), however, the drawbacks of the organic devices, described in the previous section, limit their application to neuromorphic hardware. Extensive work has been done by the scientific

community to study the potential of perovskite devices for ultra-low power consumption neuromorphic applications.

One significant advantage of hybrid perovskites compared to their organic counterparts is their excellent light absorption properties, which allow them to interact with the light-forming photonic artificial synapses. Photonic synapses are emerging technologies due to their larger bandwidth, faster signal processing, and lower power consumption compared to traditional electrical stimuli [32]. In general, the hybrid perovskite synaptic transistors that have been reported in the scientific literature so far, have achieved synaptic functions, only when they are stimulated by light or by both light and electrical stimuli simultaneously. In practice, in these works, HPs have mainly served as floating gate layers or form heterojunctions with organic materials to absorb light and separate charges, in photonic three-terminal synaptic devices, as discussed extensively in chapter **2.2.2.4**. Pure hybrid perovskite materials have rarely been applied directly to transistor channels to severe as active material [33] [34], which leads to simplified device architectures and less energy consumption [35]. This is a gap in this research topic that needs to be filled, as also reported in the recent review paper of Xue et al [35].

Also, very little works exist in the literature for perovskite synaptic-transistors that work solely by electrical stimulation [36], [37], [30], so the energy consumption of those devices has not been studied extensively. Among the existing studies, the energy consumption is estimated to be higher than the biological level, as the post-synaptic current is measured in the μA range and the applied pre-synaptic voltages are set at -5V, -20V, -30V for the references [36], [37], [30] respectively. Additionally, the transistor channel dimensions in these works are big, in the millimeter and centimeter order of magnitude resulting in high energy consumption (~μJ per synaptic event). Downscaling the device's dimensions to minimize the device area can further lower the energy consumption of the devices. The downscaling of those dimensions to the nano-level has not been reported by any work in the literature for synaptic transistors, so far, being also an open topic for further research. Downsizing of the device is also difficult, when perovskite material is used as the channel material, and needs to be addressed before these devices can be densely integrated on chips.

According to the previous statements, several research gaps in scientific literature, for this topic, arise that this thesis addresses. All the above are summarized in the thesis' motivation in the next section (**1.3)**.

1.3 Thesis motivation and overview

The increasing demand for developing energy-efficient neuromorphic hardware has led the scientific community to investigate innovative materials and device configurations that can reproduce synaptic functions. Studies have shown the capability of $MAPbI_3$ perovskite memristors to replicate low-energy consumption artificial synapses, at the biological level, as discussed in the work of Xiao et al. [38], while others have shown that three-terminal synaptic transistor configurations can further reduce energy consumption, and at the same time, achieve more stable and controllable synaptic functions [39], [31].

Existing works in the literature, for incorporating perovskite in synaptic-transistor configurations, that work solely by electrical stimulation, are limited while the energy consumption of those devices has not been calculated extensively [36], [30]. This thesis investigates the fabrication and electrical characterization of synaptic-transistor devices using $CH_3NH_3PbI_3$ ($MAPbI_3$) as the channel material, setting the foundations for a better understanding of the performance and potential utilization of those devices in neuromorphic hardware applications. Leveraging the exceptional optical properties of $MAPbI_3$, such as broad spectral absorption and light-induced ion migration, the investigation of the synaptic functions is conducted through a combination of electrical and light stimulation, allowing the utilization of those devices as optoelectronic artificial synapses. This highlights a distinct advantage of three-terminal halide perovskite devices over many other types of artificial synapses, which are solely electrically stimulated. The research focuses on developing two different field-effect transistor (FET) configurations and scaling down the channel dimensions to the micro- and nano-levels using the electron beam lithography technique. This level of miniaturization, which is unprecedented for synaptic transistors, aims to achieve ultra-low power consumption and facilitate the integration of these devices into dense arrays for neuromorphic computing.

To sum up, this work addresses gaps in the scientific literature that can be categorized as follows:

1. **Miniaturization of channel dimensions**: A significant gap in the current research is the lack of studies focusing on the miniaturization of channel dimensions in synaptic transistors, which is strongly connected to lower working energy consumption. In current works in the literature, channel dimensions in the range of centimeters to micrometers are employed in perovskite synaptic transistors [30], [40], [37], [41]. This work is focused on this area, by fabricating synaptic transistors with channel dimensions in the nanometer scale

(e.g. 500nm x 100nm), using the electron beam lithography technique, demonstrating successful synaptic functions of three-terminal synaptic transistors with these reduced dimensions. This breakthrough shows promising potential for energy-efficient neuromorphic devices.

2. **Dual-mode stimulation (electric and light)**: Compared to organic synaptic transistors, which are typically only stimulated electrically, the devices in this work also respond to light stimulation. This dual-mode stimulation capability is a distinct advantage of three-terminal halide perovskite devices over many other artificial synapses [42], [40]. The ability to use both electrical and light stimuli offers a significant reduction in energy consumption and adds one further dimension to the operation of these devices [32]. The successful implementation of this dual-mode stimulation in the devices of this work showcases the potential for more efficient and flexible neuromorphic computing systems.
3. **Simplified architecture of photo-synaptic transistors**: Current literature on optoelectronic perovskite synaptic transistors often involves complex architectures such as floating-gate configurations, which at the same time are more energy-consuming [35]. The research in this work focuses on the direct use of halide perovskite (HP) materials for the transistor channels, without the need for floating-gate structures. To date, only two studies [33] [34] have explored this approach, however, the HP in both cases is blended with other materials, which also results in a more complicated process. This work significantly adds to this area of research by providing a more straightforward and energy-efficient alternative.
4. **Energy consumption study for solely electrically stimulated perovskite devices**: There is a notable lack of comprehensive data on the energy consumption of perovskite synaptic transistors that are solely electrically stimulated. Addressing this gap, this work provides detailed analysis and empirical data on the energy consumption of these devices. This contribution is crucial for understanding and optimizing the performance of perovskite synaptic transistors in neuromorphic applications.

In **Chapter 2** of this thesis, the theoretical foundations are set which are important for the interpretation and understanding of the experimental results. Firstly, the physical properties $MAPbI_3$ perovskite are discussed, focusing on the crystal structure, the carrier's transport properties, ion dynamics, and the optical properties. Furthermore, the architecture and the working principles of the synaptic devices are explained and a brief review of the existing works in the literature is presented, about the perovskite-synaptic transistors.

In **Chapter 3**, the experimental methods and techniques employed in this thesis are presented. In particular, a brief overview of the working mechanisms of the most important fabrication techniques that have been used is discussed and the detailed methods for every experimental process are given so that the work can be reproduced effectively by other researchers in the future.

In **Chapter 4**, the devices' architectures are presented, and the electrical characterization is performed on every device. Discussions about the energy consumption, the linearity of the conductance states update, and the device's interaction with the light are also presented, as well as a comparison of the performance of the different device architectures.

Finally, in **Chapter 5**, the conclusions and the outlook of this work are presented.

Chapter 2

Theoretical Framework

2.1 Physical properties of $MAPbI_3$

2.1.1 Crystal structure

Perovskites are materials described by the chemical formula ABX_3, where X is an anion (i.e. I^-, Cl^-, Br^-) and A, and B are cations (i.e. A: $CH_3NH_3^+$, Cs^+, B: Pb^{2+}, Sn^{2+}). For hybrid organic-inorganic metal halide perovskites, such as $MAPbI_3$, A-cation is organic, usually methylammonium (MA^+ or $CH_3NH_3^+$) with ionic radius $R_A = 0.18$ nm, or formamidinium (FA^+ or $NH_3CH{=}NH_2^+$) where R_A is estimated to lie in the range 0.19–0.22 nm [43]. The term "hybrid" indicates that the crystal is composed of both organic and inorganic components. The X-site is a halide anion, like iodine (I) ($R_X = 0.220$ nm), Br, and Cl ($R_X = 0.196$ nm and 0.181 nm, respectively) while cation B is a metal like Pb^{2+} ($R_B = 0.119$ nm) [43]. In a hybrid perovskite crystal, the organic cation is surrounded by BX_6 octahedra, which are connected at each corner to form a three-dimensional perovskite lattice, as shown in **Figure 2.1a**.

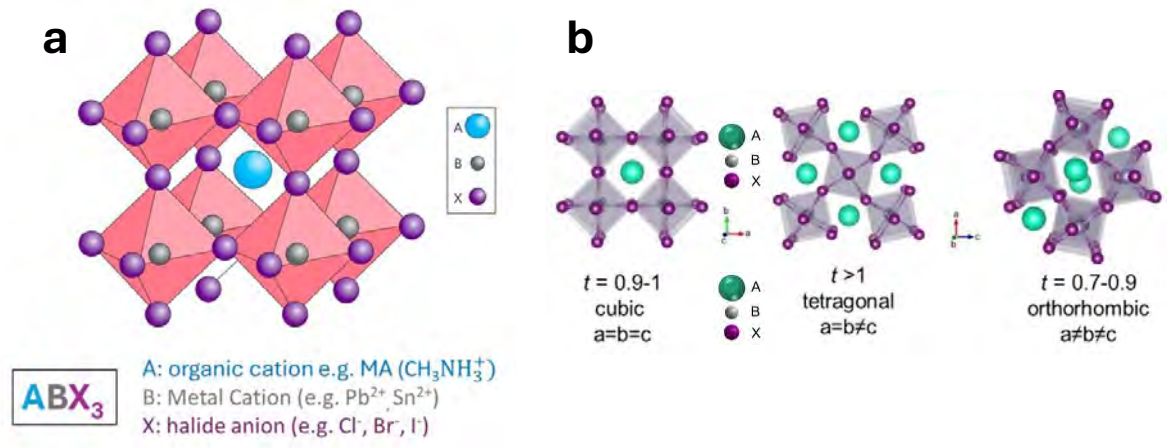

***Figure 2.1**: **a)** Cubic crystal structure of hybrid organic metal halide perovskite (HMP). Figure reproduced from ref. [43]. **b)** the three different phases of the (HMP) and associated tolerance factors. Figure taken from ref. [44].*

The crystallographic stability and potential structure of perovskite materials can be estimated by examining the tolerance factor (t) and the octahedral factor (μ). The tolerance factor (t) is determined by the ratio of distances between ions in an idealized solid-sphere model, specifically the ratio of the distance between the A and X ions to the distance between the B and X ions ($t = (R_A + R_X) / \{\sqrt{2(R_B + R_X)}\}$), where R_A, R_B, and R_X represent the ionic radii of the respective ions). A tolerance factor (t) falling within the range of 0.9–1.0 typically indicates a cubic structure, as illustrated in **Figure 2.1a**. Higher or lower values of t suggest less symmetric tetragonal or orthorhombic structures. The octahedral factor (μ) is defined as the ratio of the ionic radius of the B ion to that of the X ion (R_B / R_X) [43]. For halide perovskites (X = F, Cl, Br, I), it is generally observed that $0.44 < \mu < 0.90$ [43].

$MAPbI_3$ perovskite exhibits three different crystal symmetries: α phase (cubic), β phase tetragonal, and γ phase (orthorhombic), as shown in **Figure 2.1b** [44], [45]. At room temperature, the β-phase is stable, while a $\gamma \rightarrow \beta$ phase transition occurs at 165K and $\beta \rightarrow \alpha$ phase transition at 327K [46]. Secondary phases can also be formed, such as PbI_2, especially after the exposure of the hybrid perovskite to the humid air [47].

2.1.2 Carrier transport properties and Ion dynamics

Figure 2.2 shows the electronic band structure of the $MAPbI_3$ as calculated by DFT simulations with the PBE approximation [48]. $MAPbI_3$ is a direct semiconductor due to the direct gap formed at the R point of Brillouin's zone. The band gap energy E_0 was calculated at 1.56 eV [48].

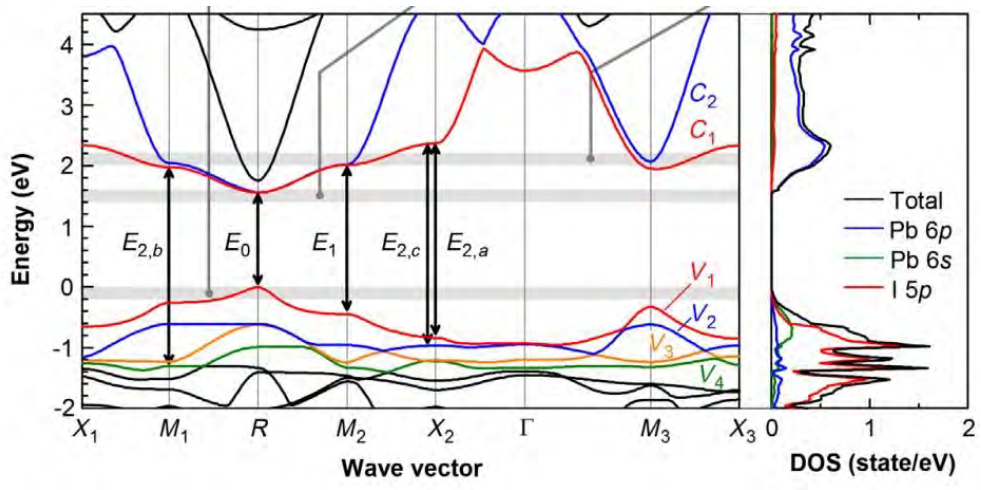

***Figure 2.2**: Band structure and DOS of the pseudo-cubic $MAPbI_3$ crystal. Figure taken from ref. [48]*

The total Density of States (DOS) and partial DOS contributions of the Pb 6s, Pb 6p, and I 5p states in $MAPbI_3$, have also been calculated as shown in **Figure 2.2** [48]. The position of E = 0V corresponds to the valance band maximum (VBM). The valence band of $MAPbI_3$ is primarily composed of Pb 6s and I 5p orbitals, while the conduction band density of states (DOS) is mainly dominated by Pb 6p orbitals [48]. An important conclusion that can be extracted from the DOS calculations reveals that C, N, and H atoms (i.e., MA^+) do not contribute to the valence band maximum (VBM) and conduction band minimum (CBM) of $MAPbI_3$. This indicates that the semiconducting properties of $MAPbI_3$ are primarily due to the inorganic component, with organic cations not participating in the formation of the valence and conduction bands. However, organic cations (MA^+) are crucial for the stability of perovskite crystals [48].

The effective mass (m*) is a crucial physical parameter that determines carrier mobility. The m_e^*/m_0 of β phase $MAPbI_3$ has been calculated with Green's function and screened Coulomb interaction approximation, or GW approximation, at 0.32 and the m_h^*/m_0 at 0.36 [49], where m_0 is the free-electron mass and m_e^* and m_h^* the effective mass for electrons and holes, respectively. The fact that the m_e^* and m_h^* have approximately equal values is quite unusual for semiconductors, while it is advantageous for carrier transport as the carrier mobility is expressed by the formula $\mu = q\tau/m^*$, where τ is the mean carrier scattering time and q is the charge. This means that both electrons and holes have relatively the same mobility.

Self – Doping

One exceptional characteristic of hybrid perovskites is the fact that they can be self-doped in contrast to most semiconductors where the doping is achieved by the incorporation of other elements in their crystal structure. Self-doping, p- or n-type can be achieved by defect engineering [50]. While in most devices vacancies typically need to be minimized for device stability, in the case of hybrid perovskites the dense vacancy generation could be advantageous for enhancing their performance in neuromorphic devices. Vacancies facilitate ion migration [51], which is essential for emulating the dynamic and adaptive behavior of biological synapses and mimicking synaptic functions.

Figure 2.3a shows the energy levels of various vacancies (V_{Pb}, V_{MA}, V_I), interstitials (Pb_i, MA_i, I_i), and antisites (Pb_I, I_{Pb}) in $MAPbI_3$. Vacancies have energy levels near the conduction band minimum or the valance band maximum, so they have low formation

energy and are therefore the most common unintentional dopants in hybrid perovskites. On the other side, most interstitial and anti-site defects have energy levels in the bandgap, forming deep traps with high formation energy (low concentration). The fact that shallow defects are far more prominent means that $MAPbI_3$ is defect-tolerant maintaining good performance and stability, without limiting the carrier transport [52]. Shallow defects can also trap the carrier and act as scattering and recombination centers but at a significantly lower rate than deep defects [52].

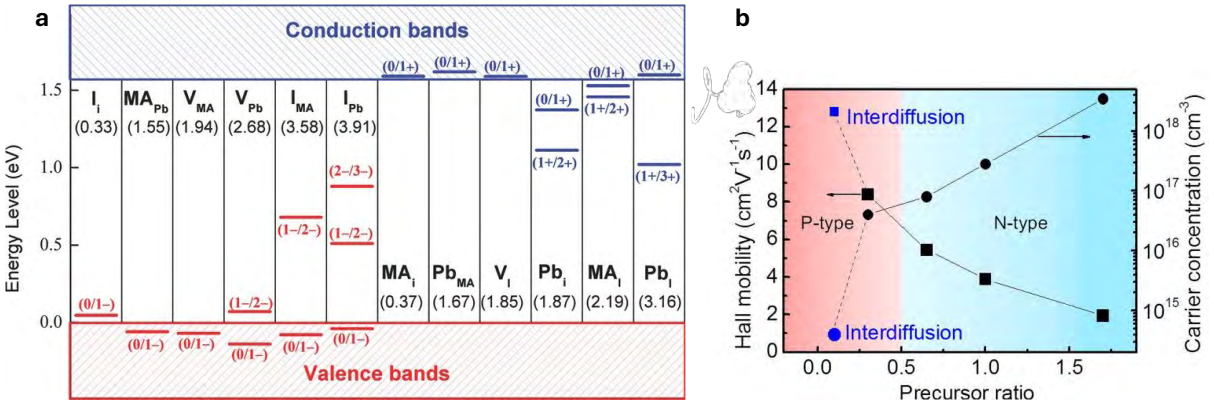

***Figure 2.3**: **a)** Calculated energy levels of point defects in $CH_3NH_3PbI_3$. The formation energies of neutral defects are shown in parentheses. The acceptors/donors are ordered by the formation energies (from left to right). Figure taken from ref. [53]. **b)** Composition-dependent carrier concentration (circle) and carrier mobility (square) in perovskite films formed by one-step pre-mixed precursor deposition (black) and two-step interdiffusion method (blue). Figure taken from ref. [50].*

$MAPbI_3$ perovskite is synthesized from a solution process where the PbI_2 and MAI precursors are mixed in a solvent, such as dimethylformamide (DMF). In **Figure 2.3b** the Hall mobility and carrier concentration are plotted as a function of precursor ratio PbI_2/MAI. The carrier type switches from p- to n-type at the 0.5 precursor ratio and the electron carrier density increases in the PbI_2-rich film. Thus, it is generally recognized that $MAPbI_3$ exhibits n-type conductivity in MAI-deficient (PbI_2-rich) films, while p-type conductivity is observed in PbI_2-deficient (MAI-rich) layers [50]. Wang et al. determined that the n-type characteristics of MAI-deficient layers are due to the formation of donors from iodine vacancies (V_I). In contrast, the p-type behavior in PbI_2-deficient layers arises from the formation of acceptors caused by lead vacancies (V_{Pb}) [50].

The perovskite defects mentioned previously (V_I and V_{Pb}) are charged defects meaning free electrons and holes can interact by Coulomb interactions with them and can be scattered (ionized-defect scattering). For this reason, a significant reduction in Hall mobility (μ_{Hall}) occurs, with increasing carrier concentration, as illustrated in **Figure 2.3b**.

Ion migration

Ion migration is an intrinsic property of hybrid perovskites, and it is the main factor behind the hysteresis in the I-V curves of perovskite photovoltaic devices. It occurs easily and quickly due to the low-activation energy of the ions and the low defects' formation energy [54]. The activation energy E_A indicates how easily ions can move when an external electrical bias is applied. In the case of $MAPbI_3$ iodine (I^-) ions have the lowest E_A (0.58 eV), compared to MA^+ (0.84 eV) and Pb^{2+} (2.31 eV) ions, suggesting vacancy-assisted diffusion of iodide ions [54]. Additionally, other species such as H^+ ions, which are the smallest in size, can influence ion migration through Frenkel defects, as the migration of H^+ ions along a transient hydrogen bond between two equatorial iodides was found to have a low activation energy value of approximately 0.29 eV [55].

Hybrid organic perovskites are synthesized from a liquid solution by the so-called "solution process", with spin-coating being the most conventionally used technique. This process results in a polycrystalline thin film. Polycrystalline materials consist of grains; thus, the formation of grain boundaries is unavoidable. Grain boundaries are the interfaces that separate the grains, which can exist in various crystallographic orientations. They are considered 2D defects in the crystal structure, and they are amorphous and disordered creating electronic trap states. Also, the daggling bonds in those regions can be bonded with impurities or point defects. In the case of $MAPbI_3$ iodine vacancies can be trapped at grain boundaries changing the local charge state. Studies have shown that grain boundaries act as an ion migration channel, as illustrated in **Figure 2.4** [56], [57]. Because of the dangling bonds in grain boundaries, the activation energy for ion migration along grain boundaries is expected to be lower than in the bulk material, as fewer chemical bonds are preserved [58].

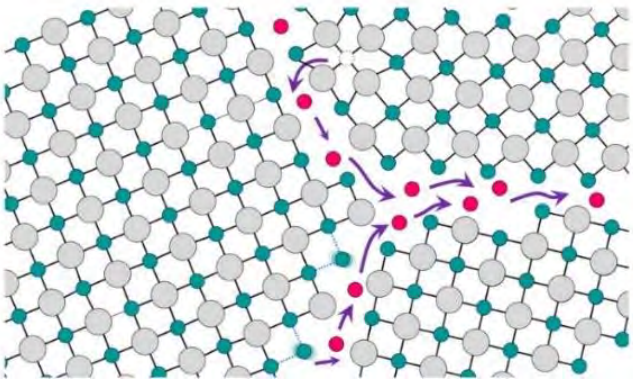

***Figure 2.4**: Ion migration channel at grain boundaries. Figure taken from ref. [58].*

2.1.3 Optical properties

$MAPbI_3$ has attracted the interest of the scientific community for applications in the field of optoelectronics, particularly for its use in perovskite solar cells. The optical properties of $MAPbI_3$ are crucial to its performance in these applications, and they are influenced by its crystal structure, composition, and intrinsic electronic properties.

$MAPbI_3$ absorbs in a broad field of the electromagnetic spectrum, covering a portion of the visible light spectrum and extending into the near-infrared. Due to this broad absorption, it is an excellent material for solar cells as it can absorb a wide range of wavelengths from sunlight. The material has an absorption onset of around 800 nm, corresponding to its direct bandgap of approximately 1.5 eV, as shown in the **Figure 2.5a**, where the absorption coefficient is plotted in function with the photon energy [59]. The direct bandgap nature of $MAPbI_3$ facilitates efficient absorption and emission processes, making it suitable not only for solar cells but also for light-emitting diodes (LEDs) and lasers.

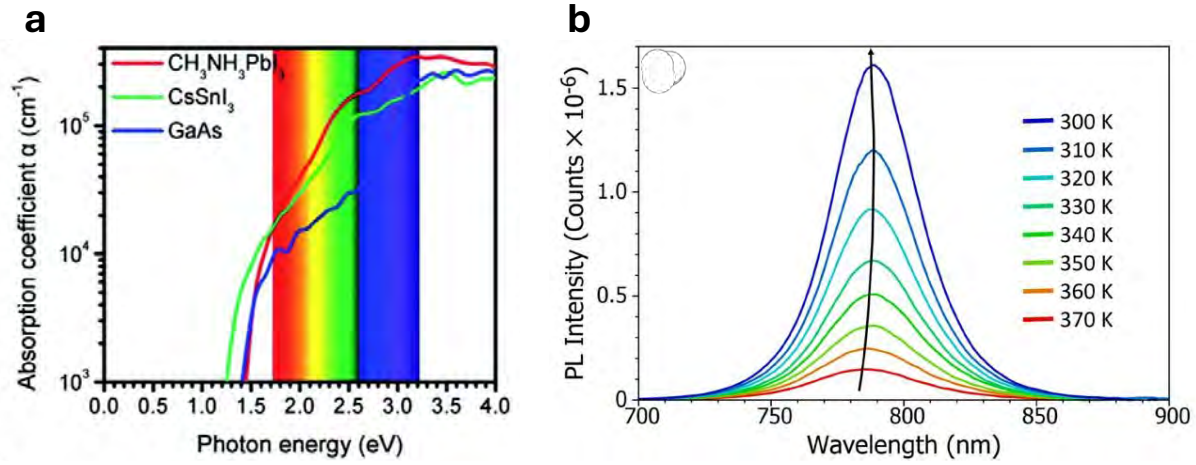

***Figure 2.5**: **a)** The calculated absorption coefficient of $MAPbI_3$, $CsSnI_3$ and GaAs materials. Figure taken from ref. [59]. **b)** The change in PL spectrum of $MAPbI_3$ over 370 K to 300 K. Figure taken from ref. [60]*

$MAPbI_3$ exhibits strong photoluminescence when excited with light of energy greater than its bandgap (~1.5 eV). The emission typically occurs around 760-800 nm, corresponding to the near-infrared region. As the temperature decreases, the PL peak narrows (**Figure 2.5b)** due to the reduced population of phonons, leading to less homogeneous broadening of the PL caused by phonon coupling at lower temperatures. Additionally, the peak wavelength of the PL redshifts as temperature decreases (**Figure 2.5b**), suggesting that the bandgap of the perovskite narrows (decreases in energy) as the temperature decreases [60]. This trend arises from

decreased orbital splitting as the lattice expands, and changes in the electron-phonon coupling [61].

2.2 Synaptic Devices

Artificial synapse devices mimic the function of biological synapses, which are the junctions through which neurons communicate in the brain. These devices are crucial for the development of neuromorphic computing systems, which aim to replicate the efficiency and functionality of the human brain. The most important function of synapses, which is also related to the brain's memory and learning mechanisms, is synaptic plasticity, meaning the strengthening or weakening of the connection between the pre-synaptic and post-synaptic neurons.

Synaptic plasticity is described by the synaptic weight. High synaptic weight means a strong connection between the pre- and post-neurons and vice versa. The alteration of the synaptic weight (ΔW) by an external stimulant can be quantitatively represented by the transition of the conductivity of the artificial synapse. Therefore, the control of the conductivity by adjusting the form of the synaptic plasticity is a goal of an artificial synapse.

2.2.1 Memristors

Memristors are devices that have shown they can function effectively as artificial synapses. They are, in general, two-terminal devices that exhibit memory resistance, meaning their resistance changes based on the history of voltage and current applied to them, which appears as hysteresis in the I-V characteristics. A typical two-terminal hybrid perovskite memristor configuration is shown in **Figure 2.6a**. It typically consists of the perovskite layer sandwiched between two metal electrodes.

In **Figure 2.6b,** a characteristic I-V curve is depicted when a voltage bias is applied to the electrodes of a memristor. Hysteresis is observed and a high resistance state (HRS) region, the red curve in **Figure 2.6b**, is separated from the low resistance state (LRS), green curve. SET voltage indicates the applied voltage which sets the memristor to the LRS, while the RESET voltage sets it back to the HRS. SET/RESET voltages, HRS/LRS ratio, endurance (how many times the memristor can be SET to LRS and RESET to HRS before it starts to fail or its performance deteriorates), retention (the ability of the memristor to maintain a given resistance

state, either HRS or LRS, over an extended period without losing information), and power consumption are critical characteristics [24].

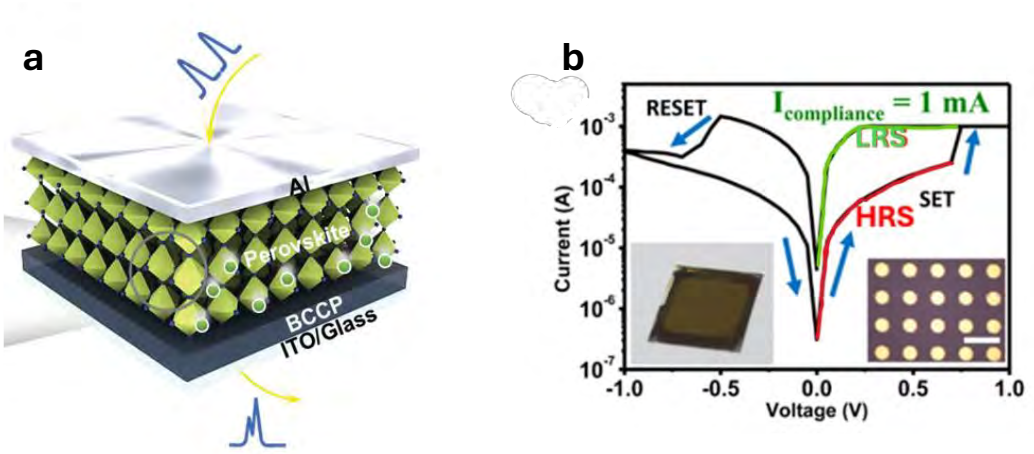

Figure 2.6: a) *Schematic representation of perovskite memristor. Figure taken from ref. [62].* ***b)*** *I-V characteristic of perovskite memristor. The low resistance state (LRS) and the high resistance state (HRS) are highlighted with green and red color respectively. Figure reproduced from ref. [63]*

Figure 2.7 illustrates how the memristor can be analogized to a biological synapse. In a biological neuron, an action potential reaches the presynaptic membrane, leading to an influx of Ca^{2+}, which triggers the release of neurotransmitters and temporarily enhances synaptic transmission [64]. In this context, the top and bottom metal electrodes of the memristor can be analogized to pre-synaptic and post-synaptic neurons (**Figure 2.7**).

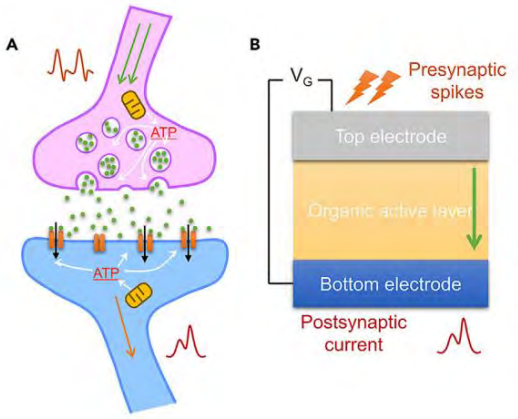

Figure 2.7: *Schematics of a biological synapse and a 2-terminal artificial synapse. Figure taken from ref. [29].*

Neurons communicate using electrical impulses known as action potentials or spikes. So, the study of memristors as artificial synapse devices involves characterizing these memristors using electrical pulse measurements. The focus is on the emulation of synaptic weight plasticity, in this case meaning the access to different conductance states. An input voltage

pulse is applied to the pre-synaptic electrode, as shown in **Figure 2.7**, and the resulting post-synaptic current, which exits through the post-synaptic electrode, is measured [65].

In **Figure 2.8a** below the post-synaptic current is plotted which rose after two pre-synaptic pulses on a $MAPbI_3$ memristor. The post-synaptic current increases after each pulse and then decays rapidly over time. This decay is caused by the change in electronic conductance of the hybrid perovskite film which is caused by the back-diffusion of ions after the pulse was removed [65].

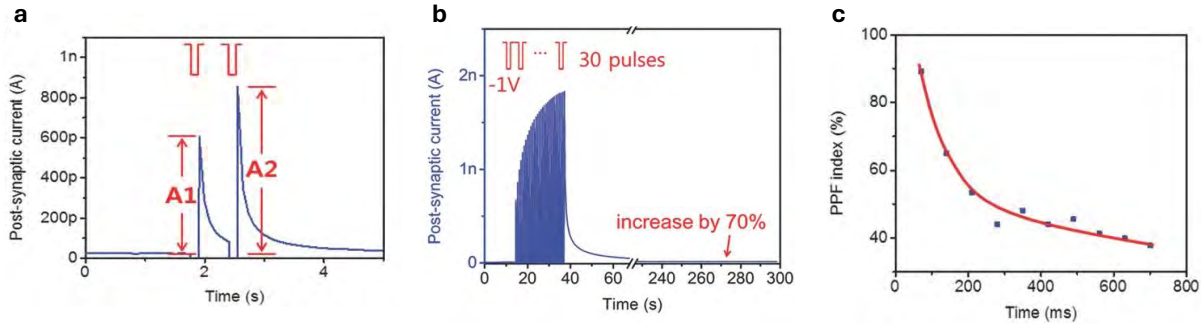

***Figure 2.8**: **a)** Synaptic enhancement achieved by two successively applied pulses, emulating a biological process of PPF. **b)** Long-term potentiation (LTP) achieved by the application of several consecutive pulses to the artificial synapse. **c)** PPF index versus time interval between successive pulses. Figures taken from ref. [65].*

Short-term potentiation (STP) is a temporal change of the synaptic strength which then returns to its initial state. One of the most well-known STP mechanisms is the paired-pulse facilitation factor (PPF) by which two pulses are applied, closely to each other, as shown in **Figure 2.8a**. The PPF factor is calculated as the ratio:

$$PPF = \frac{A_2}{A_1} \times 100\%$$

where A_1 and A_2 are the post-synaptic current values after each pulse. If $PPF > 100$ there is a potentiation in the synaptic current of the second pulse compared to the first one, while if $PPF < 100$ the synaptic current is depressed in the second pulse. The PPF factor depends on the pre-synaptic pulse frequency as shown in **Figure 2.8c**. In particular, PPF decreases as the time interval between the two pulses increases, which is also how biological synapses function [66].

If the intensity of the stimulus is strong enough, STP can be converted into LTP. The application of several presynaptic pulses within a short period causes a significant increase in current, as depicted in **Figure 2.8b**. Also, although this increased current decayed over time, it eventually stabilized and remained constant for a prolonged period. This effect is referred to as

LTP. The synaptic enhancement is approximately 70% higher compared to the resting current level, as noted in **Figure 2.8b**. This finding aligns with the characteristics of biological long-term memory [65].

Memristive mechanisms

The exact mechanism of the memristive behavior is still under debate in perovskite memristors. Generally, the memristive mechanisms of memristors can be broadly categorized into filamentary and interface-type resistive switching (RS). In the filamentary mechanism, an electrochemically active metal such as silver (Ag) or copper (Cu) is used as one of the electrodes, while an inert metal such as platinum (Pt) or gold (Au) is used as the other electrode [67]. When a positive voltage is applied to the active metal electrode, metal ions are generated through electrochemical oxidation. These ions (e.g. Ag^+ ions) migrate through the insulating layer, due to the applied electric field and are reduced, typically at the inert electrode by capturing electrons, leading to the formation of conductive filaments (CFs), as illustrated in **Figure 2.9**. As the CFs bridge the electrodes, the memristor switches to a low-resistance state (LRS), **Figure 2.9c**. Conversely, applying a negative voltage dissolves the CFs, returning the memristor to a high-resistance state (HRS), **Figure 2.9d** [68].

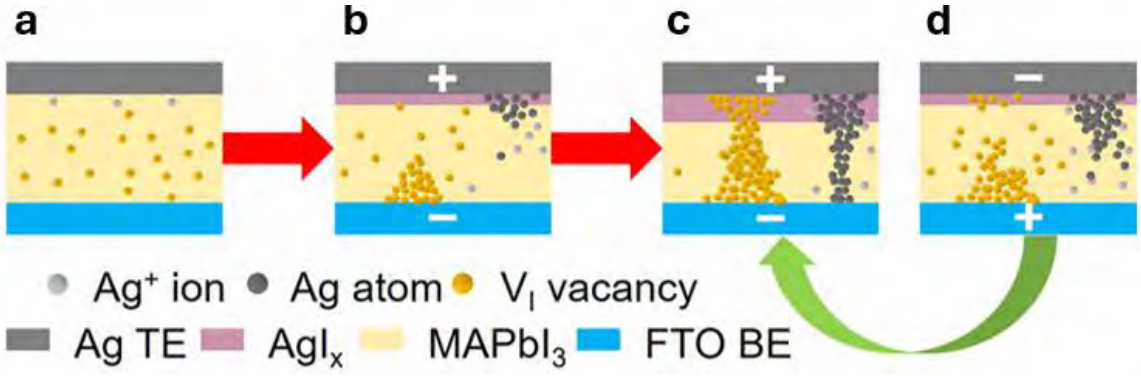

***Figure 2.9**: Double-filament model of resistive switching behaviors in the Ag/MAPbI₃/FTO memristor device. **a)** The initial state, **b)** forming, **c)** SET to low-resistance state (LRS), and **d)** RESET to the high resistance state (HRS) process of the Ag/MAPbI₃/FTO device with comparatively thin MAPbI₃. Figure taken from ref. [68].*

In OHP-based memristors, both iodine (I^-) and methylammonium (MA^+) ions can also migrate under an electric field. **Figure 2.9** illustrates the double-filament model in the Ag/$MAPbI_3$/FTO memristor device. During the SET process, iodine ions of the perovskite migrate toward the inert FTO electrode creating iodine vacancies (V_I) and forming CFs, while Ag^+ ions of the silver electrode also migrate in the same way creating Ag CFs, setting the device to the low-resistance state (LRS), as illustrated in **Figure 2.9**c [68]. During the RESET process, the iodine

vacancies are filled, disrupting the CFs and increasing resistance, high-resistance state (HRS), as depicted in **Figure 2.9d**.

Interface-type mechanism, on the other hand, relies on the modulation of the Schottky barrier at the interface between the insulator and the metal electrode. This modulation is typically caused by charge trapping/de-trapping or anion migration near the electrode interface. The contact resistance changes accordingly, which modulates the device's resistance state. As shown in **Figure 2.10a-II,** when a positive voltage is applied to the Au electrode, the Schottky barrier is reduced, enabling hole injection from the Au electrode and their capture by interfacial trapping centers. This causes the Fermi level of the material to shift towards the valence band, further lowering the Schottky barrier. Consequently, the contact between the material and the Au electrode becomes quasi-ohmic, switching the memristor to a low-resistance state (LRS). Conversely, when a negative voltage is applied to the Au electrode, **Figure 2.10a-IV** the holes are released from the trapped states. This increases the Schottky barrier, returning it to its original state, and the memristor switches back to a high-resistance state (HRS) [69], [70].

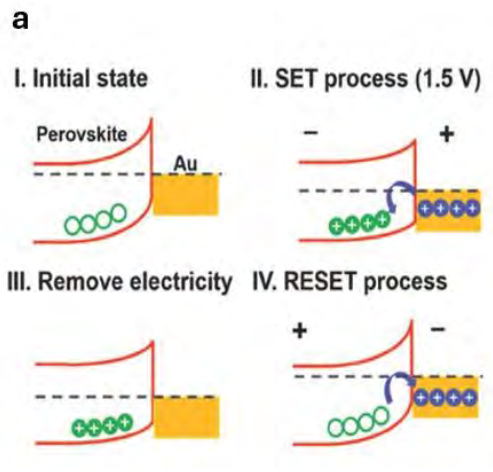

***Figure 2.10**: **a)** Electrical switching including four states: (I) initial state corresponding to HRS: hole trapping centers located at the perovskite surface; (II) SET process: hole trap states are filled, shifting the Fermi level to the valence band; (III) remove electricity: a lowered barrier and quasi ohmic contact result corresponding to LRS; and (IV) electrical reset: holes are extracted from the trap states and a transition from LRS to HRS occurs. Figure taken from ref. [69]*

2.2.2 Synaptic – transistors

While the 2-terminal memristor has a simple structure and is easily scalable, it shows some disadvantages. The memristive mechanisms show stochasticity and significant noise, they are also power-consuming and relatively slow [30]. Also, as the ions diffuse back to their equilibrium state, in absence of an external electric field, the ion migration mechanism exhibits poor long-term plasticity. Furthermore, due to the intrinsic electronic conductivity of

perovskites, a parasitic leakage current is observed in 2-terminal devices, limiting the number of achievable conductance states [30]. To overcome those issues, a new idea has arisen, i.e. the three-terminal synaptic transistor, based on the field effect transistor configuration. The working mechanism provides significant advantages related to the improved stability and controllability of the synaptic characteristics and reduced energy consumption [71], as will be discussed later.

2.2.2.1 Field Effect Transistor configuration and working principles

To understand the working principles of the synaptic transistor, it is important to introduce the field effect transistor (FET) configuration. The field effect transistor architecture is shown in **Figure 2.11a.** The gate electrode, which is usually a metal or a highly doped silicon substrate, is isolated from the rest of the device by a dielectric layer, which serves as an insulator. Above this dielectric layer, the source and drain electrodes are positioned, with a defined separation between them that determines the channel length. The semiconducting layer, deposited over the source, drain, and gate structure, functions as the channel through which current flows [72].

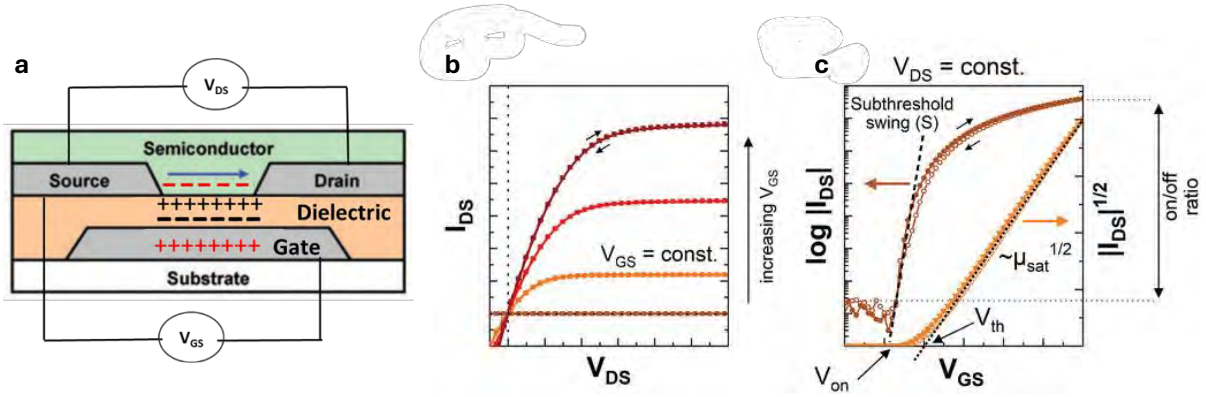

***Figure 2.11**: **a)** schematic cross-section of a field effect transistor. In this case a positive gate bias is applied on the gate electrode and negative charges are accumulated in the channel. Figure taken from ref. [73]. **b)** Output characteristics (sweeping V_{DS} while V_{GS} = const.) for an ideal field-effect transistor. c) transfer characteristics (sweeping V_{GS} while V_{DS} = const.) Figures taken from ref. [74].*

Voltage is usually applied to the gate electrode (V_{GS}) and the drain electrode (V_{DS}). The source electrode is normally grounded (Vs = 0). When a voltage bias is applied to the gate and source electrodes, the dielectric is polarized, and an electric field is generated in the channel. The corresponding charge carriers of the semiconductor are accumulated on the dielectric/semiconductor interface (for example negatively charged carriers are accumulated when a positive gate bias is applied, as shown in **Figure 2.11a**). In this way the conductivity of this channel can be modulated by the gate bias, controlling the current flow between the source and drain electrodes.

In **Figure 2.11b-c** the current-voltage characteristics are depicted. As shown in **Figure 2.11b**, where a constant gate bias is applied and the drain-source voltage sweeps, the channel's conductance can be modulated for different values of the gate voltage. Also, in the **Figure 2.11c,** where a constant drain-source voltage is applied and the gate voltage sweeps, there is a threshold gate voltage value, V_{TH}, where if the gate voltage exceeds this value, the current increases rapidly, and the channel becomes more conductive. Below the threshold voltage, no current flows through the channel. The above functions allow the FET to act as a switch or amplifier in electronic circuits, with the gate bias having a key role in controlling the channel conductance. Detailed information considering the transistor characteristics can be found in the paper of Zaumseil et al. [72].

When a perovskite material is used as a channel material, the mobile ions, can also be attracted in or repelled out of the interface of the perovskite/insulator, when a gate bias is applied, as it is schematically represented in **Figure 2.12a.** Those ions screen the gate electric field, limiting its effect on the electronic charge carriers (electrons or holes) and reducing their mobility. For this reason, the characteristics of the perovskite transistor, at room temperature, are not expected to be like the conventional characteristics of the **Figure 2.11b,c.** Chin et al. [75] fabricated a $MAPbI_3$ ambipolar field effect transistor and showed that a high electron and hole mobility can be achieved when the transistor operates at low temperature (78K), where the screening effects associated with the ionic transport can be reduced, as ion movement is suppressed at that temperature. At room temperature, the characteristics show a big hysteresis effect, as shown in **Figure 2.12b**, which although is something undesirable for conventional FETs applications, is extremely interesting for neuromorphic device applications, such as synaptic transistors that can work as artificial synapses.

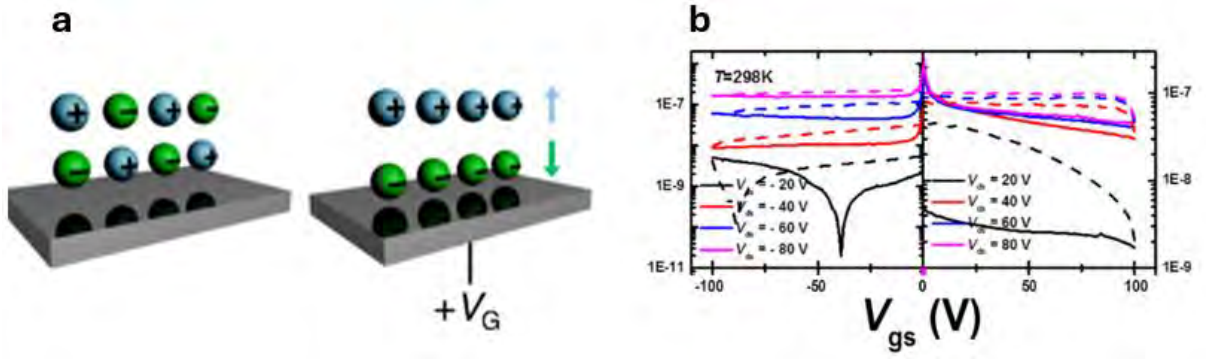

***Figure 2.12**: **a)** Schematic representation of proposed polarization mechanism of mobile ionic species in $MAPbI_3$ perovskite, under the influence of externally applied gate field (V_G). This results in screening of the gate electric field, leading to poor performance. Figure taken from ref. [76]. **b)** Perovskite FET*

output characteristics. Solid and dashed lines represent the forward and backward sweeps, respectively. Figure taken from [75]

2.2.2.2 Synaptic – transistor working principles

As mentioned earlier, synaptic transistors have the FET configuration and can benefit from the hysteresis in I-V characteristic loop, originating mainly due to ion migration, enabling access at multiple memory states for artificial synaptic memory applications [40].

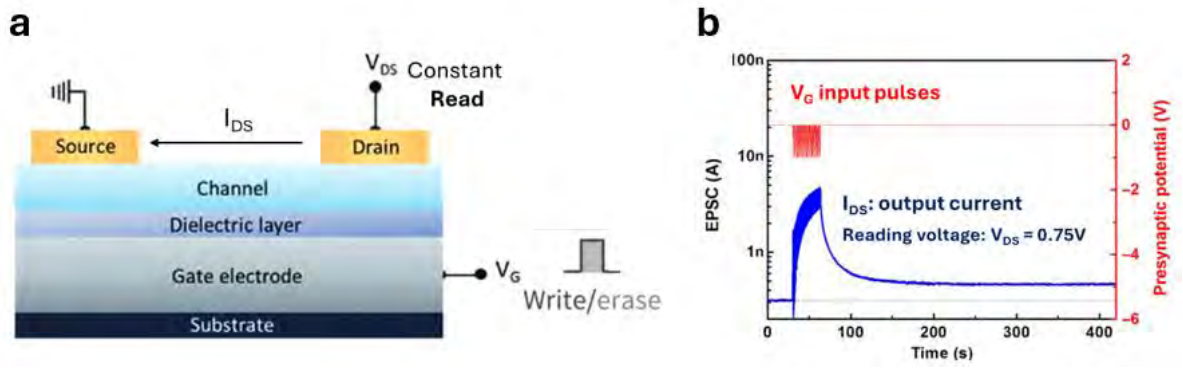

***Figure 2.13**: **a)** schematic representation and measurement protocol of synaptic transistor. Constant voltage pulses are applied to the gate electrode (writing process) and constant drain-source voltage (reading process). Figure taken from ref. [77] **b)** Postsynaptic current versus time stimulated by 30 presynaptic spikes (−1V,50ms). Reading voltage, V_{DS} =0.75V. Figure taken from [42].*

To study the performance of a synaptic transistor, constant voltage pulses are applied by the gate electrode modifying the conductance of the device by accumulating ions and electrons in the channel (writing process), as shown in **Figure 2.13a**. At the same time a low continuous drain-source voltage is applied to measure the synaptic current (I_{DS}) of the channel (reading process), as shown schematically in **Figure 2.13a**.

Figure 2.13b shows a characteristic pulse measurement, on an organic core-sheath nanowire synaptic transistor, where 30 presynaptic gate pulses of -1V and 50ms duration are applied. The postsynaptic current is measured by applying a V_{DS} = 0.75V [42]. The post-synaptic current increases after each voltage pulse, reaching 15 times higher in the last pulse compared to the resting current. After the end of the gate pulses, the current of the channel stays 1.5 times higher than the resting current, indicating the LTP mechanism [42].

A depression of the post-synaptic current can also be achieved by applying opposite value gate pulses, 1V and 50 ms duration, as shown in the **Figure 2.14a**. The plot of the excitatory post-synaptic current (EPSC), which is the I_{DS} current of the channel, in the function of the pulse number is frequently used for the study of artificial synapses, as shown in **Figure 2.14b**. It can be seen that various conductance states can be accessed after each pulse, emulating the synaptic plasticity of biological synapses.

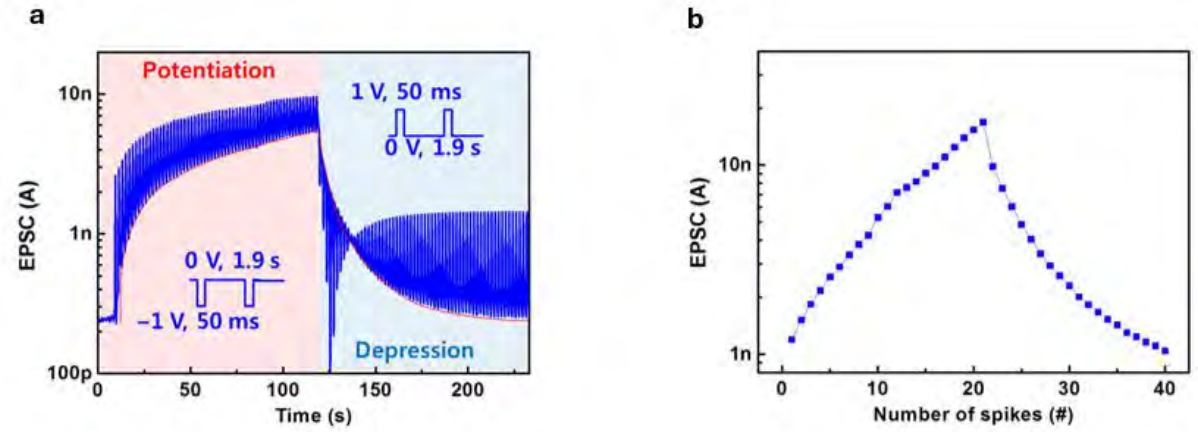

***Figure 2.14**: **Long-term synaptic plasticity (LTP)**. **a)** Postsynaptic current triggered by 60 negative and 60 positive pulses. **b)** Postsynaptic current as a function of nonlinear presynaptic spikes. Figures taken from [42]*

While there are multiple works of electrolyte-type organic synaptic transistors [31], [42], [78], [79], little attention has been paid to perovskite synaptic transistors, due to the lack of a systematic and reproducible way to control the rate of ion transport in the channel [30].

2.2.2.3 Perovskite synaptic – transistors & literature overview

The works on electrically stimulated perovskite synaptic transistors [30], [36], [37] that can be found in the scientific literature are limited, however, existing ones show the potential of the perovskite material for synaptic applications. In the work of Rogadakis et al. [36] a multi-cation perovskite is deposited as the channel material in a synaptic-transistor configuration. In their work drain-source voltage pulses are applied under a constant gate voltage. As shown in **Figure 2.15a**, the postsynaptic current is increased after each drain-source pulse, while it is further enhanced when the gate bias is also applied during the drain-source pulses in the device, leading to a 15x increase in the 20th pulse for V_G = 6V. Similar results for the influence of the gate bias on the post-synaptic current were extracted by Ma et al. who used the $MAPbI_{3-x}Br_x$ perovskite in combination with the indacenodithiophene−benzothiadiazole copolymer (IDT-BT) [37]. As is shown in **Figure 2.15b,** LTP and LTD are significantly accelerated when a negative continuous gate bias is also applied during the measurements [37].

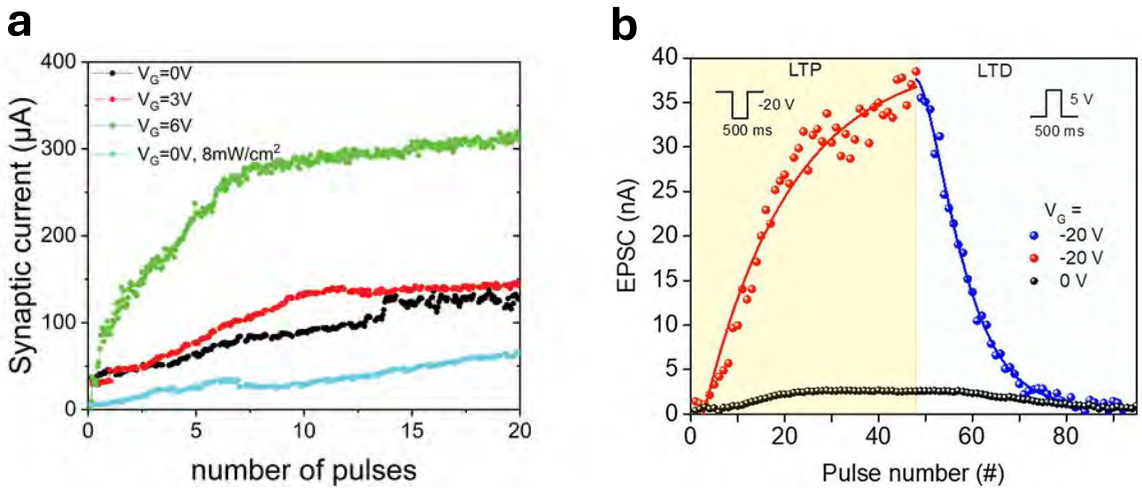

Figure 2.15: a) *Long-term Potentiation process under light and gate bias. Protocols using 20 Drain-Source pulses of amplitude of 5 V and duration of 100 ms each. Figure taken from [36].* ***b)*** *Progression plots of the EPSC under dark as a function of the number of input drain-source pulses (V_{Pot} = −20 V, V_{Dep} =5V,t_{width} = 500 ms) in dark at the different V_G values of 0 and −20 V. Figure taken from [37]*

Jeong et al. [30] used an inorganic metal halide perovskite, the $CsPbBr_3$, in a top-gate-bottom contact transistor configuration, where the gate electrode is positioned above the perovskite layer, with a ferroelectric layer separating them, and the source and drain electrodes (contacts) are situated below the perovskite layer. They showed the STP mechanism by measuring the PPF index 135% as shown in **Figure 2.16b** and the LTP and LTD (long-term depression) mechanisms as shown in **Figure 2.16a,** by applying -30V, 20 ms gate pulses for the LTP and +15V, 20ms gate pulses for the LTD.

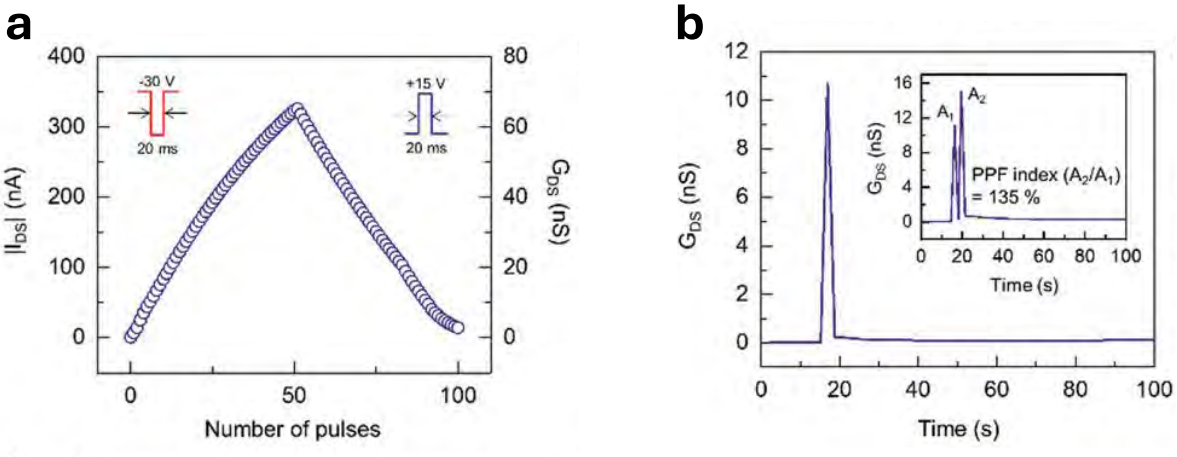

Figure 2.16*: **a)** Long-term potentiation (LTP) and long-term depression (LTD) characteristic of the perovskite transistor artificial synapse of which the channel conductance is updated by multiple pulses up to 50 times for LTP and LTD, respectively. The amplitude and width of the pulse used for LTP (−30 V, 20 ms) and LTD (+15 V, 20 ms) are represented in the inset.* ***b)*** *Short-term plasticity with a conductance update by a single pulse (−30 V for 20 ms). The inset shows a PPF characteristic with time. Figures taken from ref. [30].*

2.2.3 Photo-synaptic transistors

Photo-synaptic transistors are the bridge between neuromorphic computing and optoelectronics. Using light as an additional stimulus on neuromorphic devices could offer a new approach for tuning synaptic plasticity, potentially enhancing learning and memory abilities. Additionally, photonic synapses, are emerging as promising candidates for sensory artificial synapses due to their larger bandwidth, faster signal processing, and lower power consumption compared to traditional electrical stimuli [32]. Another advantage of photonic synapses is that they can be used directly for in-sensor computing [80].

In MHP photonic transistors, the migration of the iodine vacancy V_I is accelerated under light illumination, as reported by [32], increasing the ionic mobility. At the same time illumination prevents the formation of iodine vacancies (V_I) in $MAPbI_3$ and promotes their spontaneous annihilation, as reported by reference [81]. This can be understood as light illumination increases the formation energy of V_I and delays the formation of V_I-rich conducting regions in the perovskite film [81]. Therefore, light stimulation either in the form of light pulses or continuous light illumination proposes a different way to tune the synaptic plasticity.

The lowest energy consumption of optoelectronic artificial synapses has been recorded by Zhu et al. [82] who fabricated a Black phosphorus (BP)/CdS heterostructure-based artificial photonic synapse with multilayer BP as a conducting channel and CdS flake as a light-sensitive layer. They achieved energy consumption of 4.78 fJ per light pulse and 25 fJ per voltage pulse [82].

In the case of $MAPbI_3$ photo-synaptic transistors, most of the previously reported devices primarily focus on the floating-gate structure, where metal halide perovskites (MHPs) typically function as the floating-gate layer for trapping charges, while the semiconductors deposited on top of perovskites act as the channel layer for charge transport. Synaptic devices with this floating-gate structure generally offer benefits such as long-term memory retention and a gate-tunable effect. However, the multilayer material deposition process complicates fabrication. Moreover, the thickness of the upper sedimentary material affects the light absorption capabilities of MHPs. Additionally, when MHPs are used as the conduction layer, their overall charge conductivities are often relatively low, especially if the gate effect cannot be achieved [33]. Consequently, a relatively high operation voltage is usually required to produce a sufficiently high response current, leading to increased electrical energy consumption, in the range of pJ to nJ per synaptic event [83], [84], [85].

An example of a floating-gate photo-synaptic transistor is illustrated in **Figure 2.17:**. It is a substrate-as-gate transistor configuration, where the Si substrate acts as the gate and the SiO_2 layer as the gate dielectric. A poly(vinylpyrrolidone) (PVP), $CsBi_3I_{10}$ perovskite blend was employed to form the hybrid dielectric layer for charge capture, acting as a floating gate, and PDPP4T was deposited on the top to form the semiconductor layer [86].

These devices can demonstrate interesting synaptic functions, like LTP and LTD. Light pulses of 0.3 mJ/cm^2 intensity and 0.2 s duration increase the post-synaptic current demonstrating the LTD mechanism, while gate voltage pulses cause the depression of the current demonstrating the LTD mechanism, as shown in **Figure 2.17b**.

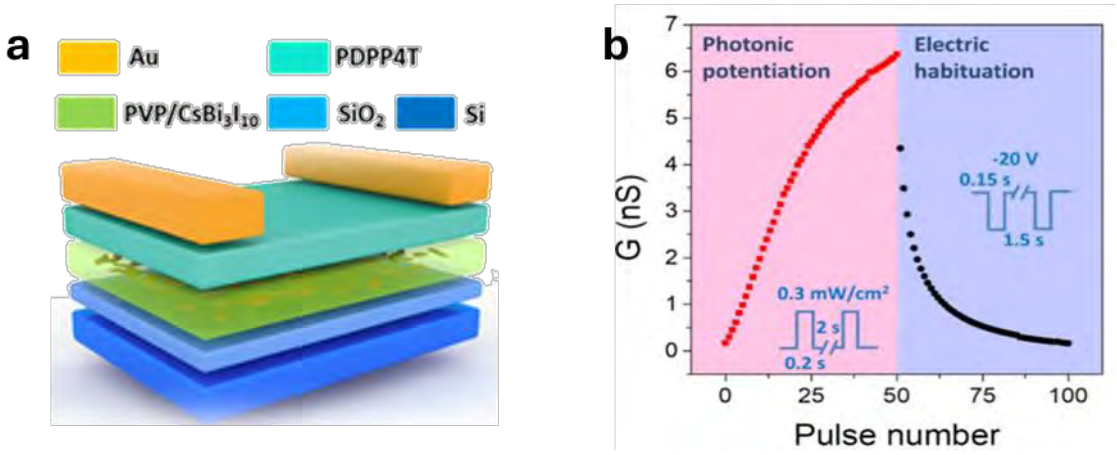

Figure 2.17: ***a)*** *Schematic of the $CsBi_3I_{10}$-based organic synaptic transistor.* ***b)*** *Potentiation−depression curve obtained by 50 consecutive light pulses (430 nm, 0.3 mW cm^{-2}, 0.2 s duration, 2 s interval) and 50 negative electric pulses (−20 V, 0.15 s duration, 1.5 s interval). Figures taken from ref. [86].*

The mechanism can be clearly understood by the schematic representation depicted in **Figure 2.18**. In the initial stage (**Figure 2.18a**), light illumination generates a large amount of electron-hole pairs and excites electrons from the valence band of $CsBi_3I_{10}$, to the conduction band. Since the HOMO level of PDPP4T (−5.2 eV) is higher than the valence band of $CsBi_3I_{10}$ (−5.9 eV), photogenerated holes from $CsBi_3I_{10}$ can transfer to PDPP4T, leaving behind photogenerated electrons and preventing their recombination with holes, due to the band mismatching between the PVP/$CsBi_3I_{10}$ and the organic semiconductor layer (PDPP4T) (**Figure 2.18b**). The trapped photogenerated electrons also induce an additional electric field accelerating the holes to escape into the PDPP4T layer [41]. The trapped electrons in the floating-gate layer can be released by applying a negative gate bias, by breaking through the barrier, as shown in **Figure 2.18c**. This causes the injection of the holes back to the floating gate (PVP/$CsBi_3I_{10}$), and the recombination with the electrons occurs [86].

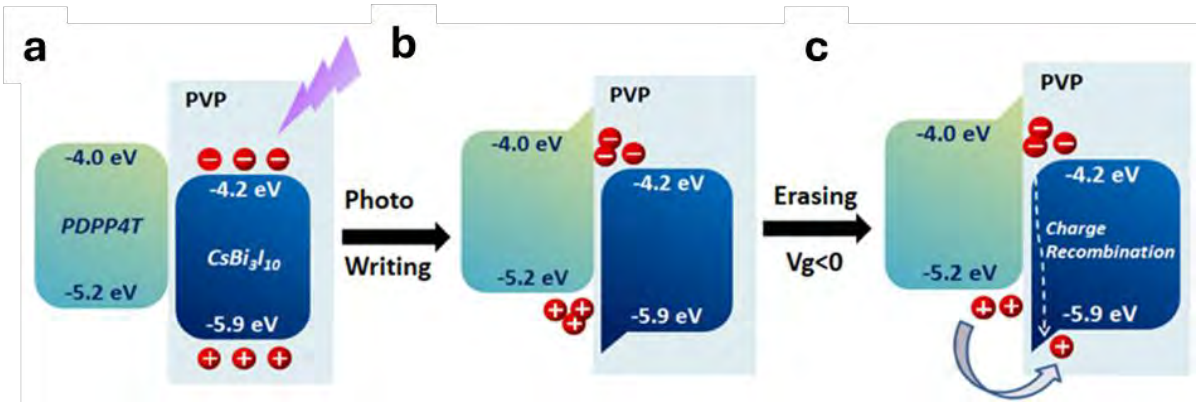

Figure 2.18: a) *Energy-band diagram of the organic synaptic transistor at the initial state.* ***b)*** *Energy-band diagram of the organic synaptic transistor after light illumination.* ***c)*** *Energy-band diagram of the organic synaptic transistor after electric erasing operation. Figure taken from [86].*

Park et al. [87] have developed an optical synapse by integrating a 2D layered MHP, serving as a floating gate, with a transparent oxide semiconductor, indium zinc tin oxide (IZTO). To simulate potentiation, the device was exposed to fifty consecutive optical spikes (100 mW/cm², 1 s) with varying wavelengths. For simulating depression, fifty consecutive positive gate pulses (20 V, 2 s) were applied (**Figure 2.19a**). When optical spikes at λ = 660 nm were used, the post-synaptic current (I_D) gradually increased from 10 pA to 300 pA, and the post-synaptic current (I_D) returned to its initial state after the application of positive gate pulses. With optical spikes at λ = 365 nm, the change in I_D for both potentiation and depression increased significantly, achieving a large dynamic range of approximately 10^4 [87].

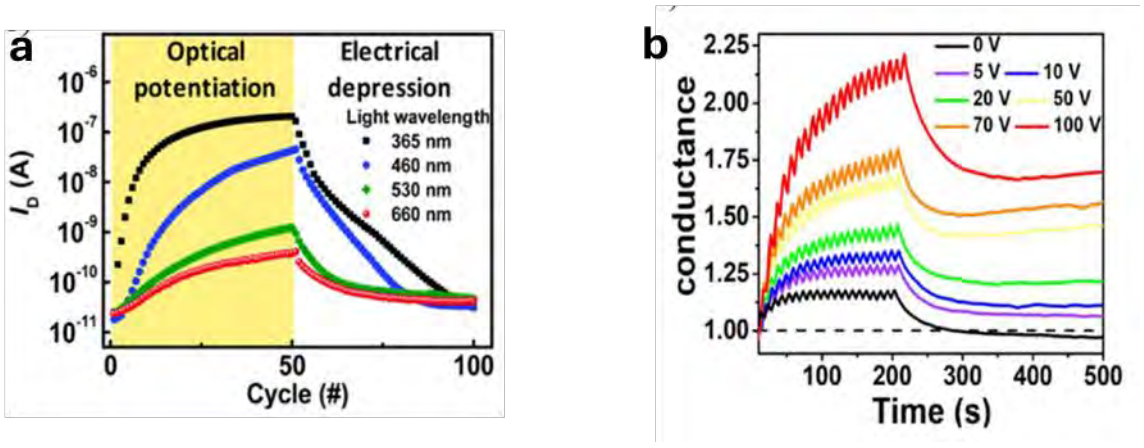

Figure 2.19: a) *Potentiation and depression characteristics of the ITZO/2D layered OIHP device. 50 optical spikes (100 μW cm^{-2}, 1 s) with different wavelengths were applied for the potentiation process and 50 positive V_G pulses (20 V, 2 s) were applied for the depression process. Figure taken from ref. [87].* ***b)*** *Gate-dependent transient characteristic of the device after application of 20 optical pulses (on and off time of 5 and 5 s, respectively). Figure taken from ref. [88].*

Pradhan et al. [88] fabricated a photonic synaptic transistor with graphene-perovskite quantum dots (G-PQD) superstructure as the active medium and observed a gate-dependent LTP, when

the gate bias is also applied during the light pulses, as shown in **Figure 2.19b** [88]. As the gate voltage becomes more positive, the increase in conductance due to photogenerated carriers under illumination is enhanced. The same happens to the retention capability after the light is removed, as the current does not decay to its original state (**Figure 2.19b**) [88].

The only photo-synaptic transistor with $MAPbI_3$ perovskite as the semiconductor material has been reported by Yin et al. [85]. In this work they fabricated a silicon nanomembrane (Si NM) synaptic-transistor, as Si NM is well known for ultralow energy consumption for Si-based devices such as transistors. A low energy consumption was achieved at 1 pJ per synaptic event [85].

Hao et al. [33] reported a perovskite photonic synaptic transistor without the floating gate, based on $CsPbBr_3$ quantum dots blended with organic semiconductor DPP-DTT. They reported energy consumption as low as 0.5 fJ per synaptic event, which is the lowest among perovskite photonic synaptic transistors, showing that MHPs are promising for developing photonic synaptic devices with ultralow spike voltage and power consumption. However, the device showed degradation after 1 week of exposure to the air [33].

Chapter 3

Experimental Methods & Techniques

3.1 Overview of Processing and Fabrication Techniques

The synaptic transistor devices developed in this study adhere to a field-effect transistor configuration, comprising a multilayer structure with various materials, including metal for contacts, dielectric for gate electrode insulation, semiconductor for channel material, and polymer for device encapsulation. Consequently, the fabrication process requires a variety of techniques and methods, presenting significant challenges, particularly downscaling the devices to the nano-level. Thorough cleaning of the substrates and contamination control in the atmosphere is extremely important to ensure the minimization of contaminants such as particles and organic residues, as they can generate defects and poor adhesion of the overlying deposited layers. This requires the fabrication of devices in a cleanroom environment to minimize the introduction of particles or impurities. A summary of the different techniques utilized in this work for every transistor's component is shown in **Figure 3.1**.

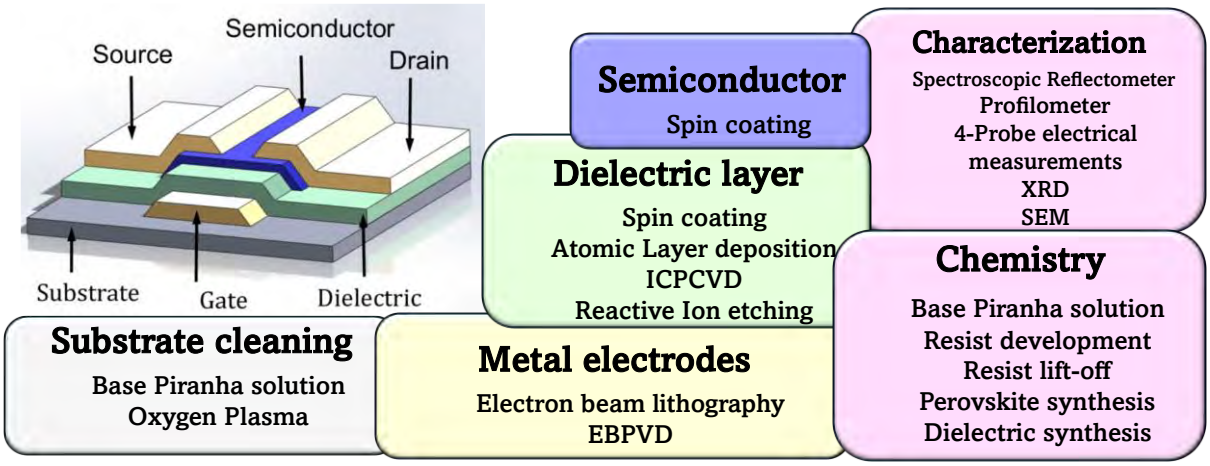

Figure 3.1: *Overview of the experimental methods and techniques employed for fabrication and characterization of each component in the transistor configuration. (Top-left) Field effect transistor architecture and notation of its components.*

3.1.1 Electron Beam Lithography

Electron beam lithography (EBL) is a widely used technique for writing nanostructures (e.g. the electrodes of the nano-transistors) on different substrates. The electron source has the advantage, compared to the conventional photolithography technique, of extremely high resolution, making the writing of nanoscale features possible, with the downside of being significantly slower. It is therefore commonly used in research lab settings and for prototyping. EBL takes place in a high vacuum chamber using high-energy electrons ranging from 10 to 100 keV. The essential components include the electron beam source (also known as the electron gun), the column that contains the electromagnetic lenses and apertures, and the chamber itself, as shown in **Figure 3.2a.**

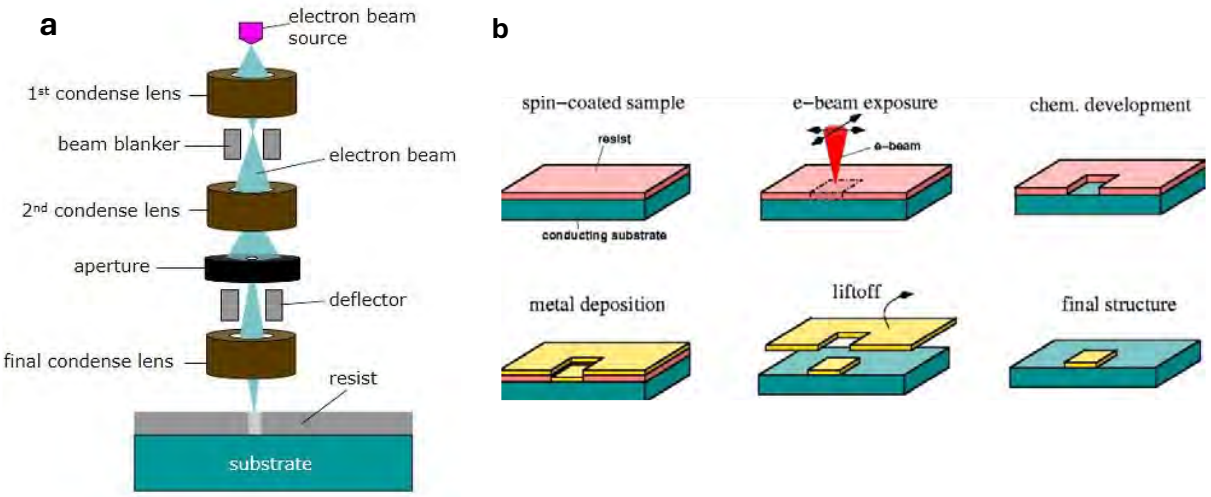

***Figure 3.2**: **a)** Side view of electron beam lithography setup. Figure taken from ref. [89]. **b)** Electron beam lithography process (spin-coating of resist, electron beam exposure, chemical development, metal deposition, lift-off). Figure taken from [90]*

In the EBL writing process, illustrated in **Figure 3.2b**, a very tightly focused electron beam exposes the resist, a polymer that is sensitive to e-beam exposure and that is typically spin-coated on the substrate. The pattern is designed by the user in a computer-aided design (CAD) or Graphic Design System (GDSII) file format and uploaded on the EBL software. The regions of the resist that have been exposed by the electron beam change their solubility, allowing the removal of those regions by a wet chemistry process (in the case of positive resists), called the development process of the resist. In this stage, the resist acts as a mask allowing thin film deposition or etching only on the patterning areas. Finally, the lift-off process follows in which the unexposed resist is dissolved in a solvent, lifting the deposited thin film layer on the top, as well. In the end, only the patterned regions remain, covered with the metal (**Figure 3.2b**).

3.1.2 Electron Beam Physical Vapor Deposition (EBPVD)

Electron Beam Evaporation (EBPVD) is a method used to deposit thin films on a substrate. An electron beam which is produced with thermionic emission of electrons, by an electric current that heats a tungsten filament, hits a solid material, placed in a crucible, causing its evaporation. The process takes place under high-vacuum.

A high voltage is applied between the filament and the hearth, accelerating the electrons toward the crucible. A magnetic field focuses the electrons to form a beam which then strikes the material in the crucible, leading to its evaporation and deposition on the substrate. When the desired thickness is achieved, a shutter covers the surface of the samples and the deposition stops. The desired film quality can be attained by regulating process parameters such as power input, gas flow rate, chamber pressure, inter-electrode spacing, reactor geometry, and substrate temperature. The EBPVD process is advantageous due to its high film density, ease of chamber cleaning, and low operational temperatures [91]. The main components of an EBPVD tool are illustrated in **Figure 3.3**.

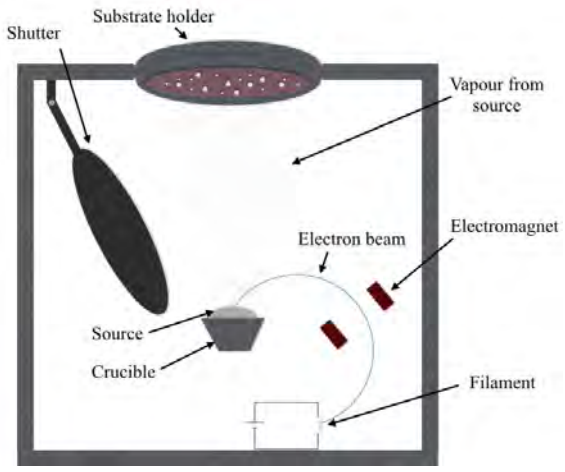

***Figure 3.3**: Schematic representation of the main components of an EBPVD tool. Figure taken from ref. [92].*

3.1.3 Inductively Coupled Plasma Enhanced Chemical Vapor Deposition (ICPECVD)

Inductively Coupled Plasma Enhanced Chemical Vapor Deposition (ICPECVD) is a low-temperature deposition technique, widely used in semiconductor technology for dielectric deposition. The advantage of this technique compared to the conventional CVD deposition technique is that the plasma that is generated in the vacuum chamber provides energy to the precursor gases. This allows for the reactions to occur, rather than having to heat the substrate to high temperatures (usually 600°C to 800°C) to drive those reactions and potentially damage

the substrate or other previously patterned/deposited structures/materials. As a result, the deposition takes place at temperatures from room temperature to 350°C. The inductively coupled plasma is a plasma source, that is generated by electric currents produced by the electromagnetic induction of time-varying magnetic fields in radio-frequency [93].

During the reaction process, the reaction gas enters the furnace cavity through the air inlet and gradually diffuses to the sample's surface. Stimulated by the electric field from the radio frequency source, the reaction gas decomposes into electrons and reactive ions. These decomposed substances undergo chemical reactions to form the initial components of the film and by-products. The initial components are chemically bonded to the sample surface, creating a solid film nucleus. This nucleus grows into islands, which then merge into a continuous film. Throughout the film growth, various by-products are gradually released from the film surface and removed through the outlet by the vacuum pump [94].

3.1.4 Reactive Ion Etching (RIE)

Reactive Ion Etching (RIE) is a plasma-based process used to etch precise patterns onto substrates, widely utilized in semiconductor manufacturing. In a typical RIE setup, the substrate to be etched is placed on an electrode at the bottom of the reactor. A feed gas is introduced into the chamber, usually CF_4 and O_2, and ionized by applying a radio frequency (RF) voltage between the lower and upper electrodes. This ionization forms plasma, and the lower electrode becomes positively charged, creating a strong electric field in the sheath region near the substrate, as illustrated in **Figure 3.4a**. The negative F^- ions in the plasma are attracted to this positive bias, accelerating toward the substrate with significant kinetic energy. As these ions collide with the substrate, they physically sputter away material from its surface, a process known as ion-driven etching, as shown in **Figure 3.4b**. Due to the electric field accelerating ions towards the surface, ion-induced etching is significantly more dominant than etching from radicals, which move in various directions, resulting in anisotropic etching. Simultaneously, reactive radicals in the plasma chemically react with the material on the substrate, forming volatile compounds that can be easily removed. The combination of physical sputtering and chemical reactions results in precise and controlled etching of the substrate. [95].

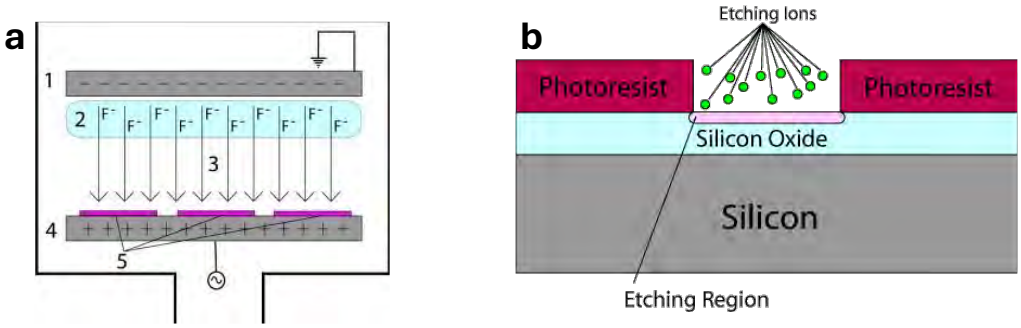

Figure 3.4: a) *Schematic representation of Reactive Ion Etching (RIE) reactor with CF_4 gas. The components are: 1: negative electrode, 2: plasma with many fluorine ions (F^-), 3: electric field created by the two electrodes, 4: positive electrode, and 5: the surface of the samples.* ***b)*** *A photoresist mask, acting as a mask, covers the Si/SiO_2 substrate, except of one uncovered region. Fluorine ions (F^-), or etching ions, accelerate towards the etching region. Figures taken from ref. [96].*

3.1.5 Atomic Layer Deposition (ALD)

ALD evolved from two methods: atomic layer epitaxy (ALE) and molecular layering (ML). In ALD, thin films are deposited using chemical gas or vapor phase species, known as precursors, in a cyclic manner. Each cycle consists of two half-cycles or half-reactions, during which up to one monolayer of a metal or metal oxide is deposited on the substrate surface.

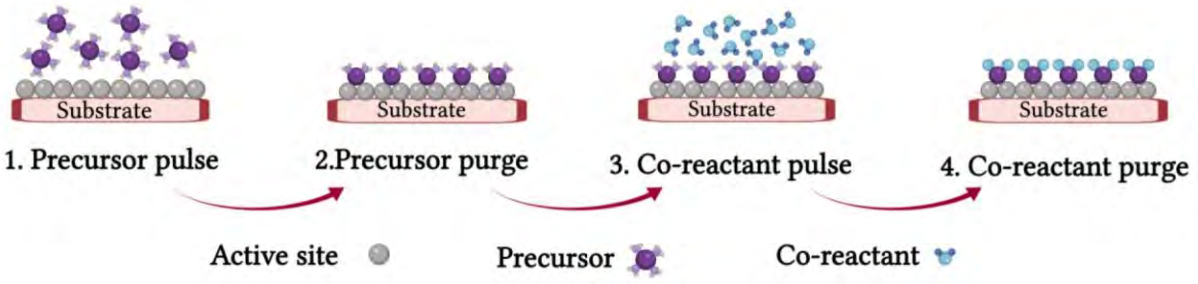

Figure 3.5*: Schematic of each ALD cycle. Figure taken from ref. [97].*

In the first half-cycle, the precursor is carried by an inert gas and pulsed into the reactor for a specific duration, reacting with the substrate's active sites and chemisorbing on the surface, **Figure 3.5-1**. Ideally, this step results in the precursor saturating the surface through a self-limiting reaction. Excess, unreacted precursor molecules are then purged from the chamber using an inert gas, **Figure 3.5-2**. In the second half-cycle, a co-reactant is pulsed into the reactor to react with the adsorbed precursor molecules on the substrate, **Figure 3.5-3**. Common co-reactants for ALD include water vapor, O_2, O_3, and NH_3. Excess co-reactant molecules and reaction by-products are purged from the reactor **Figure 3.5-4**. These two half-cycles are repeated until the desired film thickness and composition are achieved [97]. The schematic of an ALD cycle is presented in **Figure 3.5**. The growth rate is affected by the reactor temperature and pressure, pulse and purge times of the reactants, and the nature of the substrate (material

composition, surface roughness, surface preparation, such as cleaning or pre-treatment and surface chemistry).

3.1.6 Spin Coating

Spin-coating is a widely employed technique in the fabrication of thin films due to its simplicity, cost-effectiveness, and ability to produce uniform coatings. This method involves depositing a small amount of liquid precursor onto the center of a substrate, which is then rotated at high speeds. The centrifugal force generated by the spinning action spreads the liquid precursor radially outward, forming a thin layer across the substrate. An annealing step follows where the solvent is evaporated. The process is schematically represented in **Figure 3.6a**. The thickness of the resulting film can be precisely controlled by adjusting parameters such as the spin speed, spin duration, and the viscosity of the precursor solution [98]. One typical diagram of the layer thickness versus spin speed is depicted in **Figure 3.6b**.

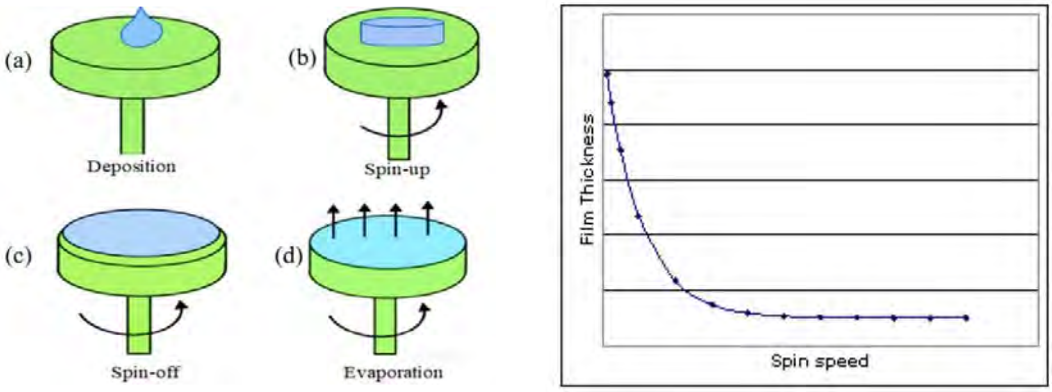

Figure 3.6: (left) *Schematic representation of a spin-coating process.* ***a)*** *The solution is deposited on the sample, and placed on a rotating disc,* ***b)*** *spinning starts at a specific speed, acceleration, and duration to achieve the desired thickness,* ***c)*** *end of the disc's spin,* ***d)*** *annealing of the sample for the solvent evaporation. Figure taken from ref. [99]* ***(right)*** *a typical plot of the layer thickness versus spin speed. Figure taken from ref [98].*

Spin-coating is particularly advantageous for creating films used in applications such as microelectronics, photonics, and surface coatings, as it ensures high uniformity and reproducibility across large areas. Moreover, the technique is compatible with a variety of materials, including polymers, ceramics, and nanomaterials, making it a versatile tool in the fabrication of advanced functional devices.

3.2 Materials & Methods

3.2.1 Materials

The chemicals used to develop patterned features after e-beam patterning were n-amyl acetate (Thermo Scientific Chemicals, 99%), o-xylene (VWR International BV), methyl-isobutyl-ketone (MBK) (VWR International BV), and isopropanol (Biosolve). Acetone was purchased from Biosolve. For the perovskite solution, PbI_2 (99.99%) was purchased from TCI Chemicals, methylammonium iodide (MAI) from Solaronix. DMF (99.8%, anhydrous) and chlorobenzene were purchased from Sigma Aldrich. 950 PMMA A8 was purchased from Kayaku Advanced Materials. For the solution of AlO_x, $AlCl_3$ was purchased from Sigma Aldrich. The positive resist CSAR 62 (AR-P 6200.09) was purchased from Allresist.

3.2.2 Substrates preparation & cleaning

In this project, 12x12 mm, p-type highly doped, Si substrates (resistivity: $\rho = 23.6\ \Omega$cm) with a 100 nm thermally grown SiO_2 layer on the top were used. The base piranha solution was employed for cleaning the substrates, as it can clean them, effectively removing organic contaminants. The substrates were placed on a Teflon holder and then submerged in a beaker with demineralized water and sonicated for 10 minutes. 50 ml of demineralized water was added to another beaker (reaction beaker), which was then placed on a hot plate and heated to 76°C. Then, 10 ml of ammonia was added, and once the temperature stabilized at 76°C, 10 ml of H_2O_2 was also introduced. When the temperature reached 77°C, the holder with the substrates was placed in the reaction beaker for 15 minutes. After the reaction, the holder was transferred to a beaker with demineralized water. Subsequently, the substrates were dipped in isopropanol (IPA) one by one and then blown dry with an N_2 gun.

Spin coating of resist & gold colloid drop-casting

The substrates were exposed to oxygen plasma for 2 minutes, for cleaning, and then heated to 150°C for 5 minutes to ensure the evaporation of water and organic residues. Each substrate was, then, placed on the spin coater and cooled by blowing N_2 with a N_2 gun. The CSAR resist was then dropped on the sample to cover its entire surface. For the CSAR, the spin-coating lasted 45 seconds with a rotating speed of 4000 rpm and an acceleration of 1000 rpm. After spin-coating, the substrates were heated to 150°C for 3 minutes. The CSAR thickness obtained was typically ~230 nm.

A droplet of a gold colloid dispersion was dropped on the corner of the substrate, which was used for focusing the electron beam during the EBL. Heating at 90°C followed to evaporate the colloid's solvent.

In this study, two different transistor configurations were fabricated, one with the substrate-as-gate design, where the substrate serves as the gate electrode and is easier to fabricate, as no lithography step is required for patterning the gate electrode. The second configuration is the bottom-gate transistor design, where a distinct gate electrode is patterned with electron beam lithography. This design offers better controllability on the measurement characteristics and is more relevant for integration of multiple transistors on a chip.

3.2.3 Substrate-as-gate device

The final architecture of the first device configuration, the so-called substrate-as-gate transistor, is depicted in **Figure 3.7**. Its name arises due to the direct connection of the gate electrode with the substrate; thus, the charge is dissipated to the whole substrate when a voltage bias is applied. It consists of a Si/SiO_2 substrate, golden gate, source and drain electrodes, a SiO_2 layer covering the parts of the sample except for the etched region of the transistor's channel, and the $MAPbI_3$ perovskite as the active material. The device is finally encapsulated with a PMMA layer. Detailed information about the experimental methods used to synthesize each component of the device is given below.

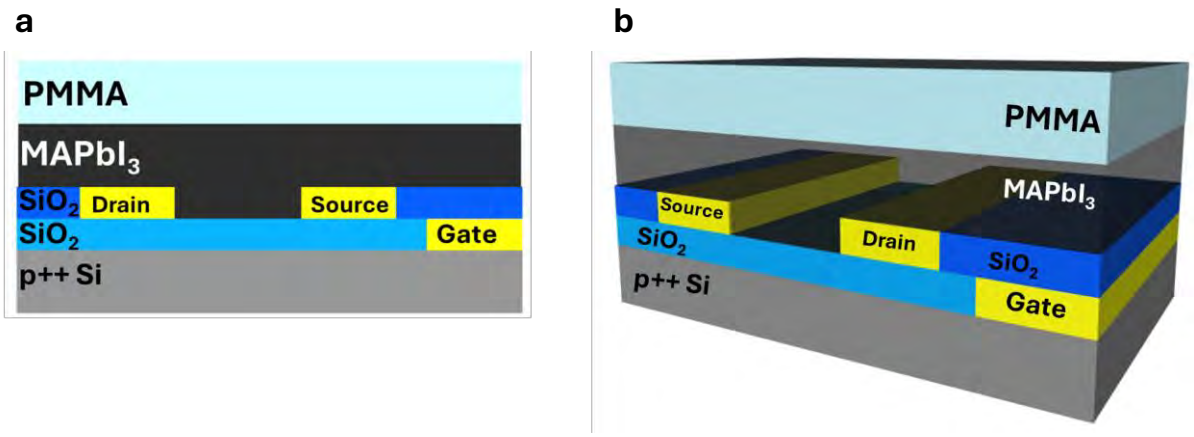

***Figure 3.7**: **a)** front-view of the substrate-as-gate transistor configuration, **b)** 3D perspective of the same device.*

Electrodes Patterning

The pattern of the features on the resist, which was deposited on the substrate as described earlier, was achieved by the E-beam lithography technique, using a Raith e-Line EBL system. In total 18 transistors were patterned on a substrate with various channel dimensions (channel

length x channel width): 1mm x 100 μm, 1 mm x 20 μm, 1 mm x 10 μm, 10 μm x 5 μm, 10 μm x 1 μm, 10 μm x 500 nm, 1 μm x 500 nm, 1 μm x 100 nm, 100 nm x 50 n. To avoid stitching errors on the patterning, the Fixed-Beam-Moved-Stage or FBMS mode was employed, where the beam remains fixed, and the stage moves. Also due to such big variations in the features' dimensions, dual beam mode was used. For patterning features bigger than 1μm, such as the contact pads, the high-beam current (HBC) of 0.85588 nA and 50 kV acceleration voltage, was used, with a 50 nm step size and area dose of 200 μC/cm^2. For the smaller features the low-beam-current (LBC) was used, of 0.1274 nA and 50 keV, with 5 nm step-size and 130 μC/cm^2 area dose.

Development of resist

Directly after the patterning of the substrates by EBL, the resist was developed by dipping the substrates one by one in n-amylacetate for 1 min, followed by 6 s in o-xylene, 15 sec in MBK: IPA 9:1 and finally rinsing in IPA. Directly, substrates were blown dry by N_2 gun and stored in a desiccator.

Metal deposition

Before depositing the metal on the patterned features, the SiO_2 layer on the sides of the substrate, which would serve as the gate electrode, was scratched off with a diamond pen to expose the substrate.

Chromium (Cr) and gold (Au) were evaporated on the samples using the Polyteknik Flextura M508 through electron-beam physical vapor deposition (EBPVD). Cr acts as an adhesion layer thus 5 nm was evaporated with Cr-soak heating mode. The deposition rate was 0.05 nm/s, the emission current 15.5 mA and the pressure of the PC chamber was 2.38e-8 mbar. The deposition of 80 nm Au layer followed, with 0.05 nm/s deposition rate, 42 mA emission current, and 1.71e-7 mbar pressure of the PC chamber. The heating mode was the Au-soak.

Lift-off

The lift-off process followed directly after the metal deposition. The samples were placed in a Teflon holder and then submerged in a beaker of acetone. The beaker was heated to 45 °C and stirred at 430 rpm overnight. Subsequently, acetone was blown on the samples with a syringe, for a more efficient removal of the gold layer, followed by dipping the samples in IPA and blow dry with N_2 gun.

SiO_2 dielectric deposition

The SiO_2 deposition was done by ICPECVD with Plasma OxfordPro 100. During the deposition, the flow rates of the precursor gases O_2 and SiH_4 were set to 32 sccm and 26 sccm respectively. The pressure of the chamber during the 30 s deposition was 2.5 mTorr and the temperature 150°C. The thickness of the layer was measured by the Filmetrics thin film analyzer as 55.96 nm. The extracted value of the refractive index was n(632.8 nm) = 1.4959 and the absorption coefficient k(632.8 nm) = 0.0000 (goodness of fit: 0.99962).

Windows patterning

For the semiconductor deposition, on the channel of the transistors, the SiO_2 should be etched on the channel. For this reason, patterning of "windows" was performed with E-beam lithography, on the regions of the transistors' channel. After the spin-coating of the CSAR according to the process described before, the EBL was done, using the high-beam current (HBC) with beam current 0.84473 nA, 50 kV acceleration voltage, step size 50 nm and area dose 200 $\mu C/cm^2$. After the patterning of the features, the development of the resist followed according to the process described before.

Etching through SiO_2

To etch through the SiO_2 the reactive ion etching technique was used, with the Oxford Plasmalab 80+. The basic standard program of "SiO_2 basic" was used, with 300 W of forward power. The gases inserted in the chamber were O_2 and CHF_3. The etching rate was calculated at 0.64 nm/s. The plasma etching was performed for 130 s with a DC bias voltage of ~ 480 V throughout the procedure. The pressure of the chamber during the deposition was 30 mbar.

3.2.4 Bottom-gate device

The final architecture of the second device configuration, the as-called bottom-gate transistor, is depicted in **Figure 3.8**. It consists of a Si/SiO_2 substrate, golden gate, source, and drain electrodes, an AlO_x dielectric layer deposited by ALD or Sol-Gel method, and the $MAPbI_3$ perovskite as the active material. The device is finally encapsulated by a PMMA layer. Detailed information about the experimental methods used to synthesize each component of the device is given as follows.

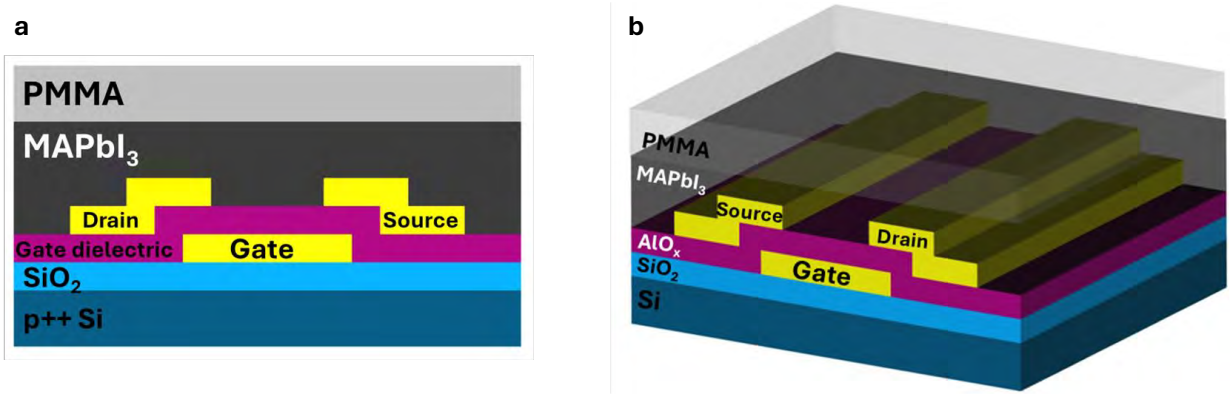

***Figure 3.8**: **a)** front-view of the bottom-gate transistor configuration, **b)** 3D perspective of the same device.*

Gate electrode patterning

The same substrates were used for this device configuration. The cleaning process and the spin-coating of the CSAR resist were done as discussed before. The gate electrode features were patterned with EBL, using only the high-beam current (HBC), with beam current 0.84969 mA, 50 kV acceleration voltage, and 50 nm step-size. The development of resist followed according to the process described before.

Metal deposition of gate electrode

Chromium (Cr) and gold (Au) were evaporated on the samples using the Polyteknik Flextura M508 through electron-beam physical vapor deposition (EBPVD). 5 nm of Cr adhesion layer was evaporated with Cr-soak heating mode. The deposition rate was 0.05 nm/s, the emission current 22 mA and the pressure of the PC chamber 2.55e-8 mbar. The 80 nm Au layer deposition followed, with 0.05 nm/s deposition rate, 44 mA emission current, and 1.43e-7 mbar pressure of the PC chamber. The heating mode was Au-soak. The lift-off process was followed as described in the previous section.

AlO_x deposition by Atomic Layer Deposition method (ALD)

Before the deposition of the AlO_x, the contact pads were covered with conducting tape. H_2O and $(CH_3)_3Al$ (TMA) were used as precursors and the carrier gas was N_2. 215 cycles were performed. The cycle was programmed to 18 ms inlet of the H_2O precursor, followed by 20000 ms delay (purge step described in **3.1.5**), 18 ms inlet of the $(CH_3)_3Al$ precursor, and 20000 ms delay (second purge step described in **3.1.5**). The temperature of the deposition was set at 150°C and the pressure of the chamber was 1.1 mbar, with 1.1 → 1.2 mbar spikes during the precursor gas inlet. The thickness was measured with the Filmetrics thin film analyzer, 29.93

nm. The extracted value of the refractive index was n(632.8 nm) = 1.6094 and the absorption coefficient k(632.8 nm) = 0.0129 (goodness of fit: 0.99954).

AlO_x deposition by Sol-Gel method

Aluminum chloride ($AlCl_3$) precursor was mixed in Acetonitrile (35%) and Ethleneglycol (65%), with a concentration of 0.2M. 0.05334 g of $AlCl_3$ was mixed in a vial with 0.7 ml of acetonitrile. The solution was stirred at 400 rpm and 70 °C overnight inside the glovebox. 1.3 ml of ethylene glycol was added outside the glovebox resulting in a 2 ml AlO_x solution. This solution was stirred on a hot plate at 400 rpm and 50 °C for 30 mins. In a separate vial, 1 ml of solvent (0.35 ml of acetonitrile and 0.65 ml of acetonitrile) was mixed.

The AlO_x solution was filtered through a 0.2 μm PTFE filter. The contact pads of the samples were covered with conductive tape. Firstly, the solvent was spin-coated on the samples at 4000 rpm speed, 1000 rpm/s acceleration, and 30 s duration, to improve surface wetting. Then the tape was removed, as it was melting when exposed to the high annealing temperature. Annealing at 250°C for 1 min followed. Then the conductive tape was adjusted again on the contact pads, followed by the spin-coating of the solution with a 2000 rpm spin speed, 1000 rpm/s acceleration, and 30 s duration. The tape was removed after the spin-coating and the samples were annealed at 250°C for 5 mins. The same process was repeated twice for a thicker layer. Deep ultraviolet irradiation followed for 5 mins and then a final annealing at 350°C for 2 hours, for the densification of the film. The thickness was measured with the Filmetrics thin film analyzer, 40.83 nm. The extracted value of the refractive index was n(632.8 nm) = 1.5748 and the absorption coefficient k(632.8 nm) = 0.0023 (goodness of fit: 0.99701).

Patterning of Drain and Source electrodes

After the spin-coating of the CSAR resist the drain and source electrodes were patterned. The FBMS, dual-beam mode was used (HBC: 0.83702 mA emission current, 50 kV acceleration voltage, 50 nm step-size, 200 $\mu C/cm^2$ area dose, LBC: 0.12464 mA, 50 kV acceleration voltage, 5 nm step-size, 130 $\mu C/cm^2$ area dose). The development of the resist was followed directly, as discussed in the previous section.

Metal deposition of drain and source electrodes

Chromium (Cr) and gold (Au) were evaporated on the samples using the Polyteknik Flextura M508 through electron-beam physical vapor deposition (EBPVD). Cr acts as an adhesion layer 5 nm of Cr, as an adhesive layer, was evaporated with Cr-soak heating mode. The deposition

rate was 0.05 nm/s, the emission current 17.2 mA, and the pressure of the PC chamber was 2.12e-8 mbar. The 80 nm Au layer deposition followed, with 0.05 nm/s deposition rate, 48 mA emission current, and 1.33e-7 mbar pressure of the PC chamber. The heating mode was the Au-soak. The lift-off process was followed as described in previous section.

3.2.5 Perovskite incorporation by spin-coating

The $MAPbI_3$ perovskite solution was mixed using methylammonium iodide **(**MAI) and lead iodide (PbI_2) as precursors and dimethylformamide (DMF) as a solvent with 40 wt% (40 wt% MAI + PbI_2 with respect to the DMF solvent). For the substrate-as-gate device, the MAI weighed 0.1622 g and the PbI_2 0.4681 g, while for the bottom-gate device 0.1618 g and 0.4677 g, respectively. The precursors were mixed in 1 ml DMF and were stirred at 400 rpm at 50°C overnight, resulting in a yellowish color solution.

The spin-coating of the perovskite was performed using an automated spin-coating robot, the "SpinBot" by SCIPRIOS [100]. The same process was followed for both device configurations. Before spin coating, the perovskite solution was filtered with a 0.2 μm PTFE filter, while the samples were cleaned with a plasma of 100W, for 1 min, using a Diener Zepto low-pressure plasma cleaner. For the spin-coating, 60 μL of perovskite solution was dispensed on the sample and rotated at 4000 rpm speed and 4000 rpm/s acceleration, for 25 sec. After the first 5 s, 0.25 μL of the chlorobenzene antisolvent was dispensed. The samples were, finally, annealed at 100 °C for 10 mins.

3.2.6 PMMA Encapsulation

PMMA was also deposited on the samples for encapsulation, by spin-coating method, using the "SpinBot". Firstly, PMMA was filtered with a 0.2 PTFE filter. For the spin-coating, 150 μL of PMMA was dispensed and the sample was rotated at 3000 rpm speed and 4000 rpm/s acceleration for 45 s. A final annealing at 100°C followed for 5 mins.

3.2.7 Capacitors

For the electrical characterization of the dielectric layers, capacitors of various electrode surface areas were fabricated. The architecture of the device consists of a Si substrate, a dielectric layer deposited on the top and patterned square Cr contact pads with dimensions 100x100 μm^2, 250x250 μm^2, and 500x500 μm^2, as illustrated in **Figure 3.9**. The detailed experimental methods of each device component are discussed in this section.

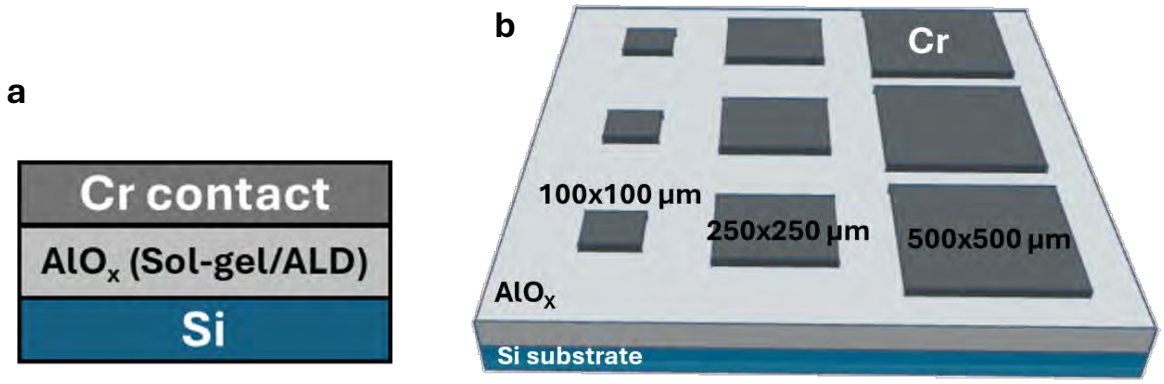

***Figure 3.9**: **a)** Schematic representation of capacitor architecture with silicon substrate as bottom electrode, Cr as the top electrode, and AlO_x synthesized with two different methods (ALD and Sol-Gel) as the dielectric material. **b)** 3D perspective of the sample with three different surface areas of the top electrodes.*

12x12 mm silicon substrates were used and cleaned with base piranha solution according to the process described in section **3.2.2.**

ALD dielectric deposition

The same process was followed as described before, for the deposition of AlOx with the ALD method. The difference was in the shorter duration of gas inlet and purge. In particular, the cycle was programmed to 18 ms H_2O, followed by 18000 ms delay, 18 ms $(CH_3)_3Al$, and 18000 ms delay. The temperature of the deposition was set at 250°C and the pressure of the chamber was 1.1 mbar, with 1.1 → 1.2 mbar spikes during the precursor gas inlet. The thickness was measured with the Filmetrics thin film analyzer, 29.93 nm.

Sol-Gel AlO_x dielectric deposition

Aluminum chloride ($AlCl_3$) precursor was mixed in Acetonitrile (35%) and Ethleneglycol (65%), with a concentration of 0.2M. 0.0269 g of $AlCl_3$ was mixed with 0.35 ml of acetonitrile in a vial. The solution was stirred at 400 rpm and at 70 °C overnight inside the glovebox. 0.65 ml of ethylene glycol was added outside of the glovebox resulting in a 1 ml AlO_x solution. This solution was stirred on a hot plate at 450 rpm and 45 °C for 1 hour. In a separate vial, 1 ml of solvent (0.35 ml of acetonitrile and 0.65 ml of acetonitrile) was synthesized.

The AlO_x solution was filtered through a 0.2 µL PTFE filter. Firstly, the solvent was spin-coated on the samples at 4000 rpm speed, 1000 rpm/s acceleration, and 30 s duration, to improve surface wetting. Annealing at 250°C for 1 min, followed by spin-coating of the solution at 2000 rpm speed, 1000 rpm/s acceleration, and 30 s duration. The samples were annealed at 250°C for 5 mins. Deep ultraviolet irradiation followed for 5 mins and then a final

annealing at 350°C for 2 hours for the film densification. The thickness of the layer was measured by Filmetrics thin film analyser, as 18.71 nm.

Electrodes patterning

Before the patterning of the electrodes with the EBL, CSAR resist was spin-coating on the samples according to the process described in a previous section. 9 square electrodes were patterned on each sample, with dimensions 100x100 μm^2, 250x250 $\mu m^{2,}$ and 500x500 μm^2, as shown in **Figure 3.9**. The HBC was used for patterning with 0.83702 mA emission current, 50 kV acceleration voltage, 50 nm step-size, and 200 $\mu C/cm^2$ area dose. After the patterning, the resist was developed according to the process described in the previous section.

Chromium electrodes deposition

Chromium (Cr) was evaporated on the samples using the Polyteknik Flextura M508 through electron-beam physical vapor deposition (EBPVD). 80 nm of Cr was evaporated with Cr-soak heating mode. The deposition rate was 0.05 nm/s, the emission current 22 mA and the pressure of the PC chamber 2.38e-8 mbar. The lift-off process followed as described in a previous section.

3.3 Characterization methods

Filmetrics Analyzer

The thickness of the dielectric layers was measured with Thin Film Analyzer Filmetrics F20 UVX which fits the thickness of a given material to the measured light reflection of the surface with a 1 nm accuracy.

Profilometer

Resist thicknesses were confirmed using a KLA Tencor Stylus Profiler P7 profilometer that can mechanically establish height differences with a sub-angstrom resolution.

Optical microscope

An optical microscope operated in a bright field mode with a magnification range of 5x, 10x, 20x, and 50x was used, at various stages of the fabrication technique, to capture images of the devices and for quality assurance checks.

Scanning Electron Microscopy (SEM)

The morphology was studied by Scanning Electron Microscopy (SEM) on a FEI Verios 460 working distance of 4.2 mm with an acceleration voltage of 5 kV.

X-ray diffraction (XRD)

For the structural characterization of the perovskite, X-ray diffraction measurements were performed on a Brucker D2 PHASER with a 1.54184 *Å* Cu K_a source. Patterns were recorded between 2θ = 5° to 2θ = 60° degrees.

3.4 Measurement methods and protocols

Transistors electrical measurements

The electrical characterization of the final devices (substrate-as-gate device and bottom-gate device) was performed with a probe station connected to an Agilent B2902A Precision/Source Measure Unit (SMU). Two channels are required for the transistor's characterization. One channel was used for the transistor's channel contacts, drain, and source, the high-force probe was placed in contact with the drain contact pad, and the low-force with the source contact pad. The other channel was used for the gate and source contacts, the high-force probe was attached to the gate pad and the low-force to the source one. Various measurements, both continuous sweeps (for the transistor's characteristics) and pulsed measurements were performed to test and optimize the devices' response.

The synaptic performance of the devices was performed with pulse measurements. Gate-source voltage pulses were applied to stimulate the conductance of the channel (writing process) and at the same time, continuous drain-source voltage was applied to read the conductance state of the channel (reading process). The minimum pulse duration was 50 ms, the minimum working limit of the instrument. The amplitude of the gate voltage pulses was mainly $\pm$5V, while in some cases in the range of $\pm$0.5V – $\pm$10 V.

For the electrical measurements under light illumination, a SOLIS-1D high-power LED, with the Thorlabs DC2200 High-Power LED Controller was used, with a maximum irradiance of 3.44 mW/mm^2 at 200 mm distance, for continuous illumination or light pulses. The LED current limit was set to 4000 mA.

Capacitors electrical measurements

For the dielectrics characterization, breakdown voltage measurements were performed on the capacitors using the probe station connected to the Agilent B2902A Precision/Source Measure Unit (SMU). Single channel measurements were performed by applying the high-force probe on the substrate and the low-force on the Cr pads. A positive voltage sweep was applied of 0 – 20V for the AlO_x -Sol-Gel dielectric and 0 – 30V for the AlO_x – ALD dielectric, with scan rates of 9.4V/s and 8.4V/s, respectively.

Chapter 4

Results and Discussion

4.1 Substrate-as-gate transistor architecture

The substrate-as-gate is one of the simplest transistor architectures that requires only one lithography step for patterning the drain and source electrodes, as the substrate has the role of the gate electrode. Thus, this architecture was the first one used to study the synaptic properties of perovskite. **Figure 4.1** describes every step of the fabrication process until the formation of the final device **Figure 4.1k,** while detailed information about the experimental methods of each component can be found in **Chapter 3**.

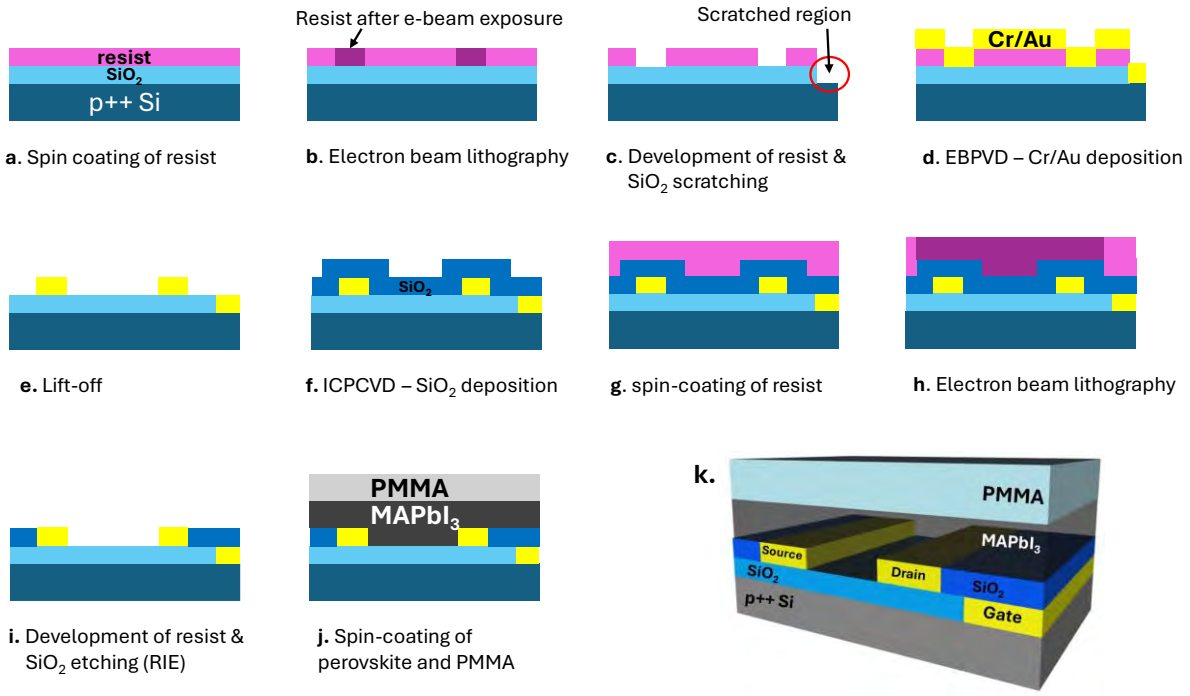

Figure 4.1: (a-j) *Schematic representation of the substrate-as-gate synaptic transistor's fabrication process.* ***k)*** *3D perspective of the final device.*

On a 12 x 12mm p-doped silicon substrate, 100 nm of SiO_2 was grown by thermal oxidation, and serves as the gate dielectric. The resist was spin-coated on the SiO_2 (**Figure 4.1a**) and the drain and source electrodes were patterned with electron beam lithography (EBL), as schematically shown in **Figure 4.1b**, followed by the development of the resist as shown in **Figure 4.1c.** An optical image of a part of the sample after the development of the resist is shown in **Figure 4.2a**. Dark lines represent the pattern of the drain and source electrodes with various channel dimensions (channel length x channel width): 1mm x 100 μm, 1 mm x 20 μm, 1 mm x 10 μm, 10 μm x 5 μm, 10 μm x 1 μm, 10 μm x 500 nm, from left to the right.

Before the deposition of the gold electrodes, the SiO_2 was scratched off on the sides of the substrate, with a diamond pen, as represented in **Figure 4.1c**. This allowed the gold to be deposited directly onto the substrate, significantly reducing the contact resistance of the probes with the substrate, during the electrical measurements. With the EBPVD technique, 5nm of Cr was deposited first as an adhesive layer and then 80 nm of Au, as shown in **Figure 4.1d**. After the lift-off, the gold remained only in the patterned regions, as shown in **Figure 4.1e** and the optical microscope image of **Figure 4.2b.**

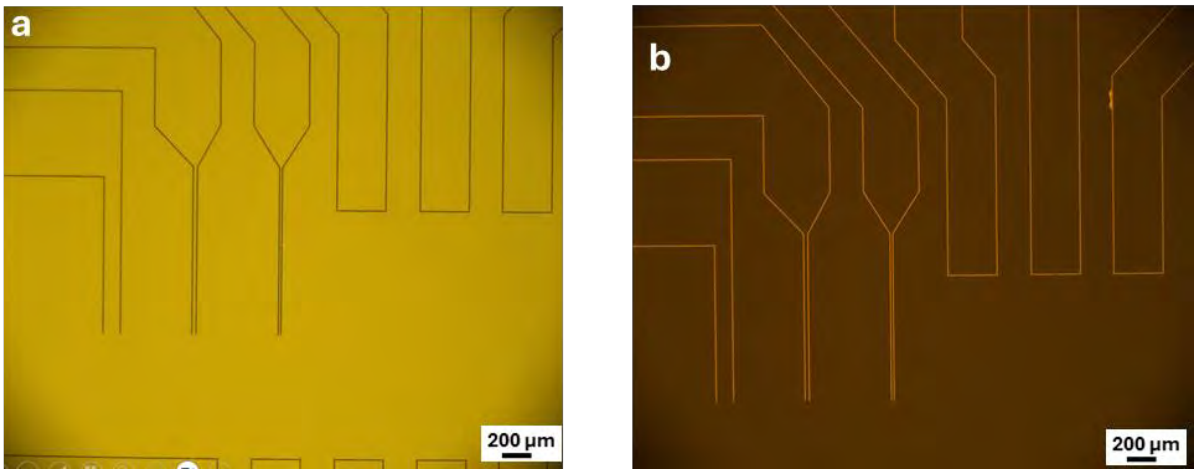

Figure 4.2: a) *optical microscope image of the sample after the electron beam lithography and the development of the resist.* ***b)*** *optical microscope image of the sample after the deposition of the gold and the lift-off process. In both images, six drain-source electrodes are depicted with channel dimensions 1mm x 100 μm, 1 mm x 20 μm, 1 mm x 10 μm, 10 μm x 5 μm, 10 μm x 1 μm, 10 μm x 500 nm, from left to the right.*

At this stage, the basic structure of the transistor has been formed (electrodes and gate dielectric) and only the semiconductor of the channel is missing for a functional transistor. However, due to the mixed ionic and electronic conductivity of the perovskite, ions can be attracted except on the channel, also on the wires, or the contact pads of the device, resulting in a parasitic capacitive current. To prevent this, all wires on the sample except for the channel

were electrically isolated, so that the perovskite will be only in direct contact with the channel. To achieve this, firstly a SiO_2 layer was deposited by the ICPECVD method (**Figure 4.1f**) and then the resist was spin-coated (**Figure 4.1g**) followed by patterning the regions on and around the channel ("windows") with EBL as shown in **Figure 4.1h**.

After the development of the resist, the SiO_2 layer, around the channel region, is etched with Reactive Ion etching (RIE). To calculate the etching rate, a Si substrate with 55.96 nm of SiO_2 deposited by ICPECVD, was etched 4 times for 20 s duration each time. The thickness of the SiO_2 layer was measured, after each etching step, with the Filmetrics thin film analyzer. The etching thickness versus etching time, are plotted in the Appendix - **Figure A6. 1.** The average etching rate was calculated to be 0.64 nm/s, so 110 s was enough to etch through the entire layer. Since the rate was not the same for each step, 20 s more was added to the etching time, resulting in 130 s, to ensure that all SiO_2 was removed.

It is noted that only the region of the developed resist is etched, as the rest region of the non-developed resist acts as a hard mask protecting the SiO_2 underneath, as illustrated in **Figure 4.1i** (more theoretical information about the RIE process can be found in **Chapter 3**). This is also presented in **Figure 4.3a-b** with the optical images, and in **Figure 4.4a-c**, with SEM images, where the dark region around the channel is the region where the SiO_2 has been etched, while the rest of the sample is covered by the SiO_2 layer.

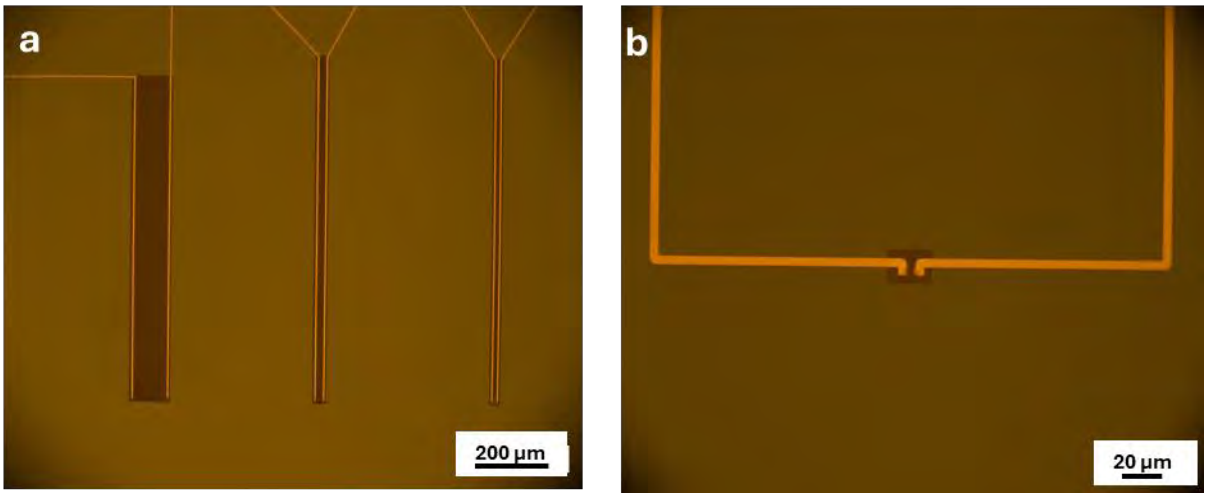

***Figure 4.3**: Optical microscope images of the channels with the etched SiO_2 windows. **a)** channel dimensions (length x width): 1mm x 100 µm, 1 mm x 20 µm, 1 mm x 10 µm from left to the right, **b)** channel dimension: 10 µm x 5 µm.*

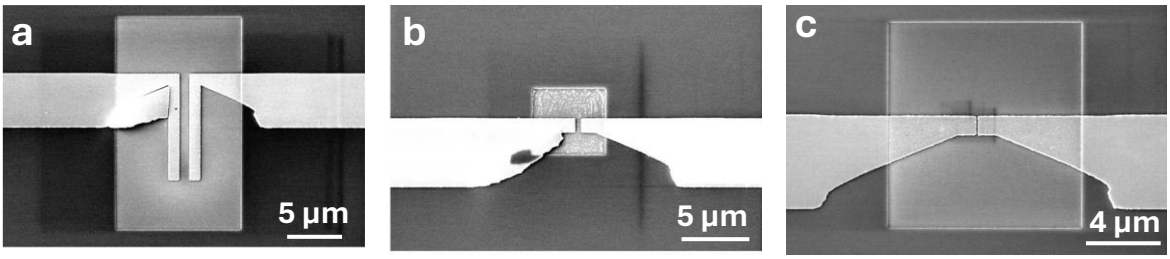

***Figure 4.4**: SEM images of the small channels with the etched SiO_2 windows. Channel dimensions (length x width): **a)** 10 µm x 500 nm, **b)** 1 µm x 500 nm, **c)** 1 µm x 100 nm.*

After the etching, the remaining resist was washed off by dipping the samples in acetone. In the end, the $MAPbI_3$ perovskite was spin-coated inside the glove box, according to the process described in **3.2.5**. Also, the samples were encapsulated by spin-coating a PMMA layer (according to the process described in **3.2.6**), as the perovskite is easily degraded by the direct exposure to the air.

4.2 Bottom-gate transistor architecture

Bottom-gate transistor architecture requires two lithography steps, one for patterning the gate electrode on the substrate and one for the drain and source electrodes on the dielectric layer. Compared to the substrate-as-gate transistor where the whole substrate serves as the gate electrode, in this case the gate electrode is distinct and limited to the channel region. This allows for better control of the channel and limits the capacitive phenomena.

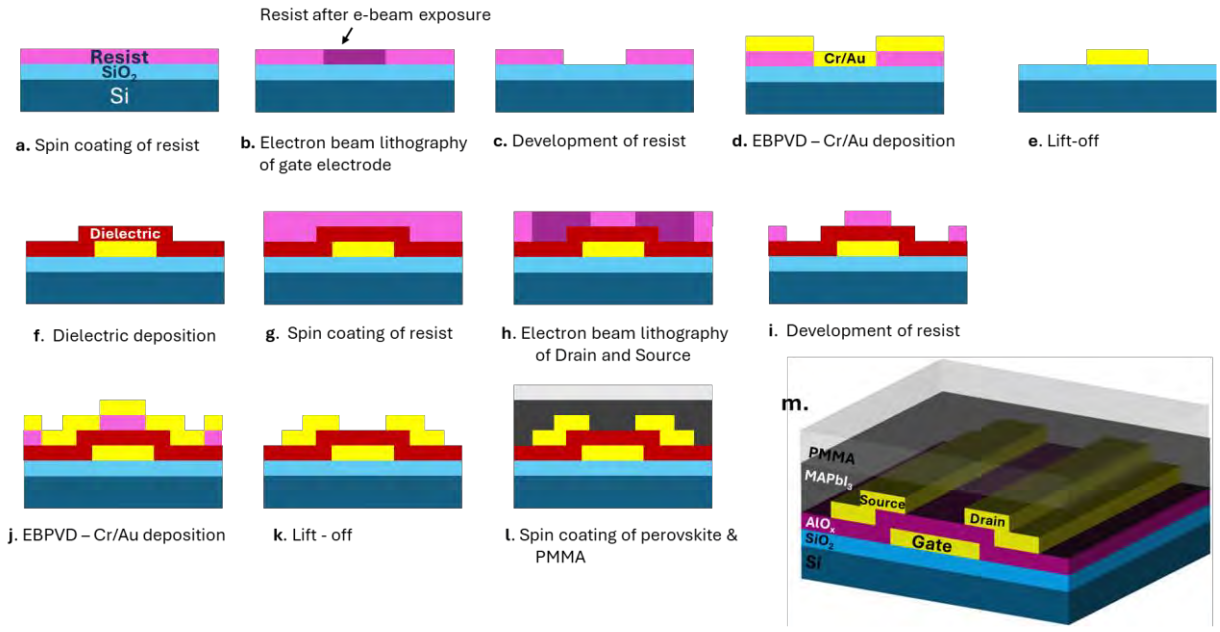

***Figure 4.5: (a-l)** Schematic representation of the bottom-gate synaptic transistor's fabrication process. **m)** 3D perspective of the final device.*

Figure 4.5 describes every step of the fabrication process until the formation of the final device**,** while detailed information about the experimental methods of each component can be found in **Chapter 3**. **Figure 4.5m** shows the 3-dimensional perspective of the device.

As shown in **Figure 4.5a**, the resist is spin-coated on the Si/SiO_2 substrate and the patterning of the gate electrode by EBL follows, as shown in **Figure 4.5b**. After the development of the resist (**Figure 4.5c**), the pattern of the gate electrodes is revealed as shown in the optical microscope image of **Figure 4.6**. The squares are the contact pads of the gate electrode, where the probes are attached during the electrical measurements. Then 5 nm of Cr is deposited on the sample followed by 80 nm of Au (**Figure 4.5d**) and after the lift-off process (**Figure 4.5e**), the excess gold is removed while it remains only on the patterned regions, as also shown in the optical microscope image of **Figure 4.6b**.

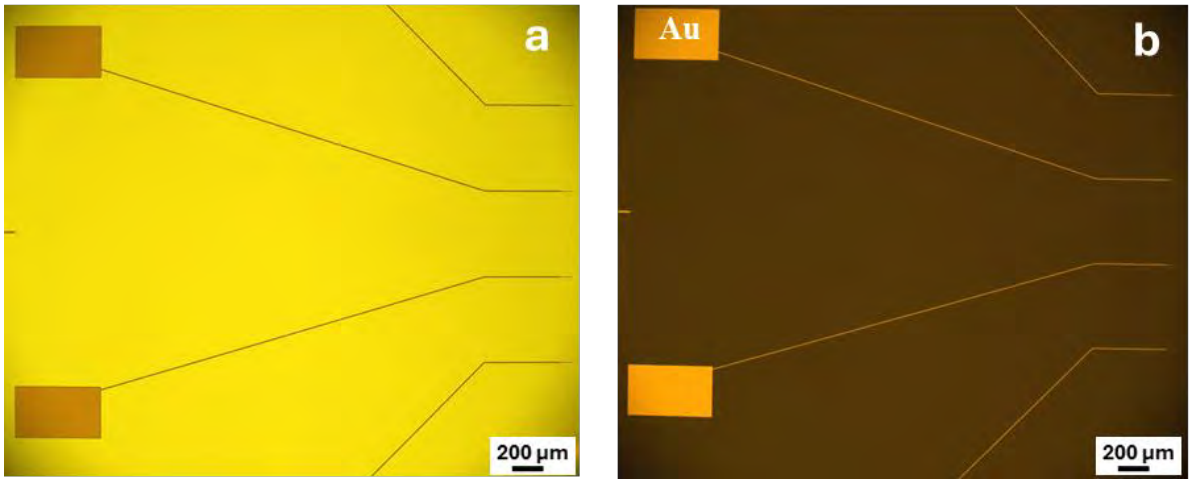

Figure 4.6: a) *optical microscope image of the gate electrodes on the sample after the electron beam lithography and the development of the resist.* ***b)*** *optical microscope image gate electrodes after the deposition of the gold and the lift-off process.*

The next step requires the deposition of the dielectric layer, for insulation of the gate electrode (**Figure 4.5f**). As a gate dielectric, the AlO_x was chosen as it has a bigger dielectric constant ($k_{AlOx} \sim 11$ [101], [102]) compared to SiO_2 ($k_{SiO2} \sim 3.9$ [103]). It is well-known that increasing k will dramatically decrease the operating voltage and the leakage current of the device [104]. Two different methods have been tested for the synthesis of AlO_x, the atomic layer deposition (ALD) and the Sol-Gel. ALD can produce Al_2O_3 films of excellent quality using a variety of metal−organic precursors and in relatively short cycle times. At the same time, the Sol-Gel method offers the advantage of a low-cost fabrication process and mass production, as the dielectric film is synthesized out of a solution. This technique has also been used by other researchers for the fabrication of $MAPbI_3$ memtransistors, with promising performance [105].

For the synthesis of Sol-Gel AlO_x the recipe of [105] was followed, but some further optimization steps were taken to improve the wetting and the uniformity of the dielectric film. The detailed experimental methods for synthesizing those films are described in **Chapter 3**. While the dielectric layer on various test samples (i.e the Sol-Gel AlOx dielectric of the capacitors) appeared to have good wetting and uniformity, in the case of the sample with the transistors the covering of the surface of the samples appeared poor, as shown in Appendix - **Figure A6. 2**. This happens due to the placement and removal of the conductive tape on the contact pads, before every annealing step during the spin-coating process, as described in **3.2.4** causing a delay between the steps. However, locally on the channel region, the film looks homogenous covering the active area of the transistor, as shown in the higher magnitude optical microscope image of figure in Appendix **Figure A6. 2-b**.

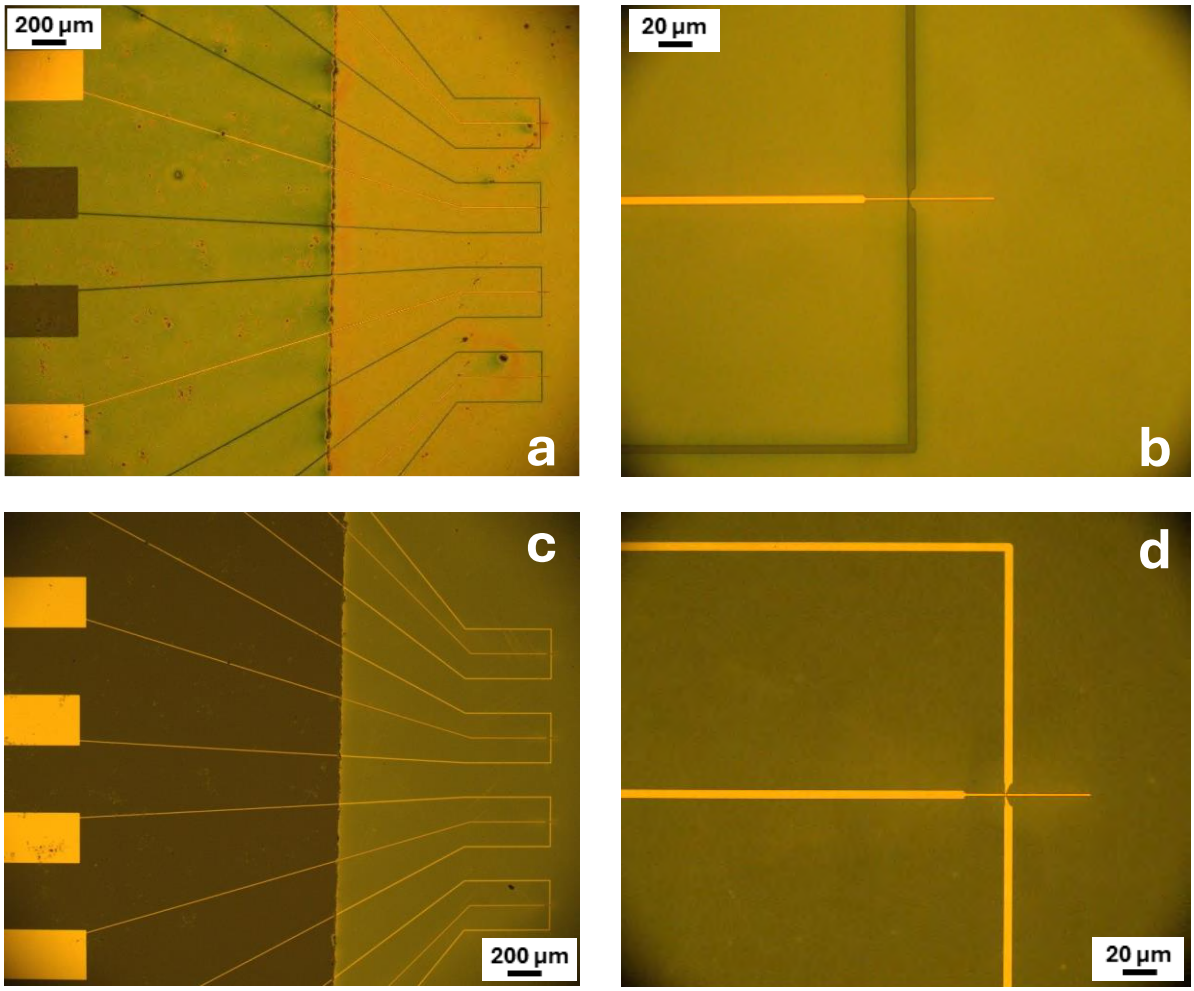

Figure 4.7: a), b) *optical images of the sample after the patterning of the drain and source electrodes.* ***b)*** *shows the region of the channel in a higher magnitude. The golden electrode in the middle is the gate electrode and the patterned features are the drain and source electrodes. The channel dimensions are 100 nm x 50 nm.* ***c), d)*** *optical images of the sample after the deposition of the gold and the lift-off process. d) shows the electrodes in higher magnitude. The channel dimensions are 100 x 50 nm.*

After the deposition of the dielectric layer, a lithography process followed, for patterning the drain and source electrodes. The resist was spin-coated (**Figure 4.5g**) and the drain and source electrodes were patterned followed by the development of the resist, as shown in the **Figure 4.5h-i** and the optical microscope image of the **Figure 4.7a**. The AlO_x-ALD dielectric layer is also noted in this figure, which covers only the region of the channels, while the region with the contact pads, is uncovered. A closer look at the 100 nm x 50 nm channel is shown in **Figure 4.7b**, where the gate electrode, of 1 μm width, is in the middle and the patterned drain and source electrodes form a gap of 100 nm, over the gate electrode, which is the channel of the transistor.

The challenging part of the drain and source electrodes' patterning was the alignment of the patterned features with the bottom pattern of the gate electrodes, meaning the gap formed by the drain and source (the channel) should be over the gate electrode, which was just 1μm wide. To achieve this, marks were patterned on the corners of the sample during the first lithography step, so that the design of the second lithography step, of the drain and source electrodes, would be aligned in reference to those marks. The marks used for this reason are the crosses shown in the Appendix - **Figure A6. 3**, at the top left corner of the sample.

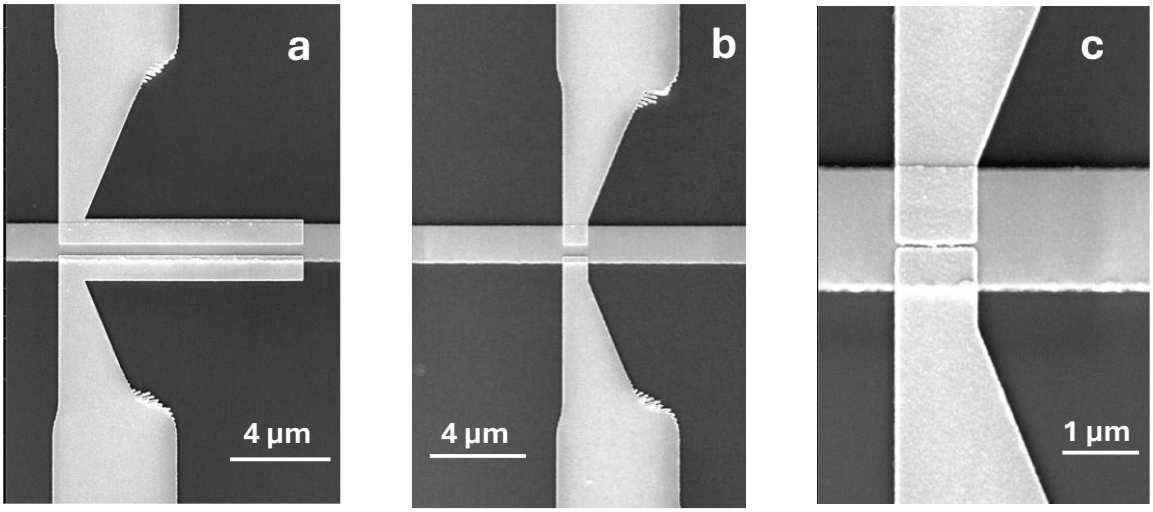

Figure 4.8: *SEM images of the electrodes. The electrode in the center is the gate electrode and the electrodes on the top are the drain and source electrodes, with the gap between them being the channel of the transistors. Channel dimensions:* ***a)*** *10 μm x 500 nm,* ***b)*** *1 μm x 500 nm,* ***c)*** *1 μm x 100 nm.*

Then, 5 nm Cr was deposited followed by 80 nm of Au (**Figure 4.5j**) and the lift-off process (**Figure 4.5k**). In the optical microscope images of **Figure 4.6c**, it can be seen that the gold remained only in the patterned regions and the drain and source electrodes have been formed. A closer look at the electrodes in the channel region is presented in **Figure 4.6d** and in the SEM images of **Figure 4.8**.

As a last step, the perovskite is incorporated into the channel of the transistors with the spin-coating method described in section **3.2.5** Finally, the sample is encapsulated with a PMMA layer deposited with the spin-coating method according to the process of section **3.2.6** .

4.3 Capacitors architecture

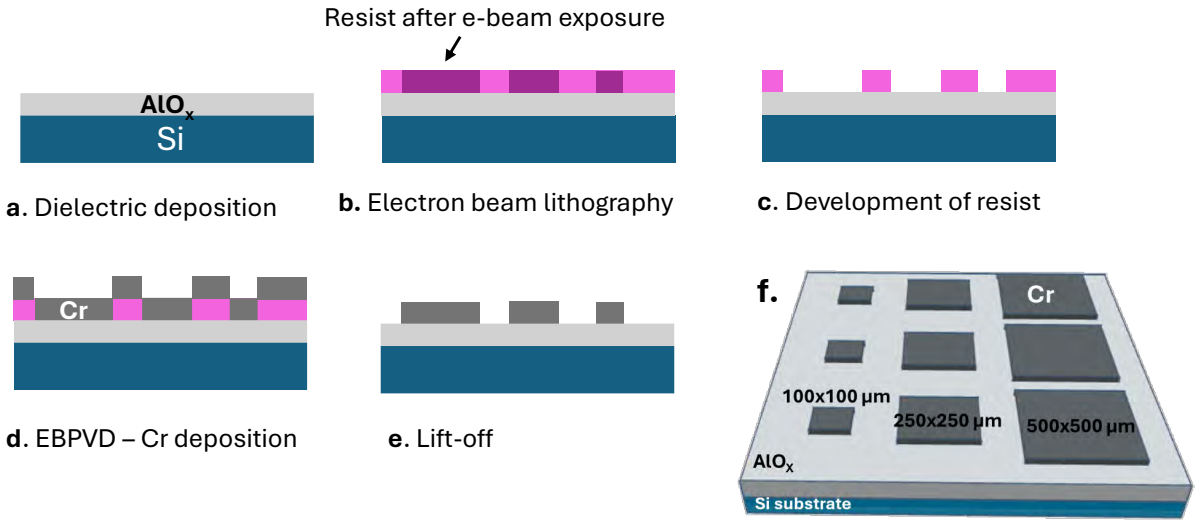

Figure 4.9: (a-e) *Schematic representation of capacitors' fabrication process.* ***f)*** *3D perspective of the final device.*

For the electrical characterization and the quality test of the dielectric layers, capacitors of various electrode surface areas were fabricated. The architecture of the device consists of a p-type highly doped Si substrate (resistivity: $\rho = 23.6\ \Omega$cm), the AlO_x dielectric layer deposited on the top, and patterned square Cr contact pads with dimensions 100x100 μm^2, 250x250 μm^2 and 500x500 μm^2. Nine contact pads were fabricated on the substrate, three of each area dimensions. The final device is shown in **Figure 4.9f**.

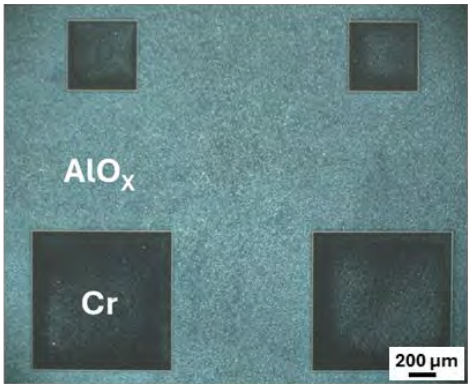

Figure 4.10: *Darkfield optical image of the Cr electrodes on the AlO_x dielectric. The dimensions of the large contacts are 500x500µm and the small 250x250µm.*

On a silicon substrate, the AlOx dielectric was deposited (**Figure 4.9a**) and then a resist layer was spin-coated (**Figure 4.9b**). The square contact pads were patterned with EBL (**Figure 4.9b**) and after the development of the resist, the Cr was deposited with EBPVD (**Figure 4.9d**). After the lift-off process the Cr contact pads were formed as shown in the dark-field mode optical microscope image in **Figure 4.10**.

4.4 Spin–coating and Characterization of Perovskite

The polycrystalline perovskite material was synthesized from a solution process. Detailed information considering the experimental methods of the perovskite deposition is discussed in **Chapter 3**. The spin-coating process is schematically illustrated in **Figure 4.11**. The $MAPbI_3$ precursor was dispensed on the samples and spin-coated at 4000 rpm for 30 s. 5 s after the start of the sample rotating, the chlorobenzene antisolvent was dispensed and finally, the samples were annealed at 100°C for 10 minutes.

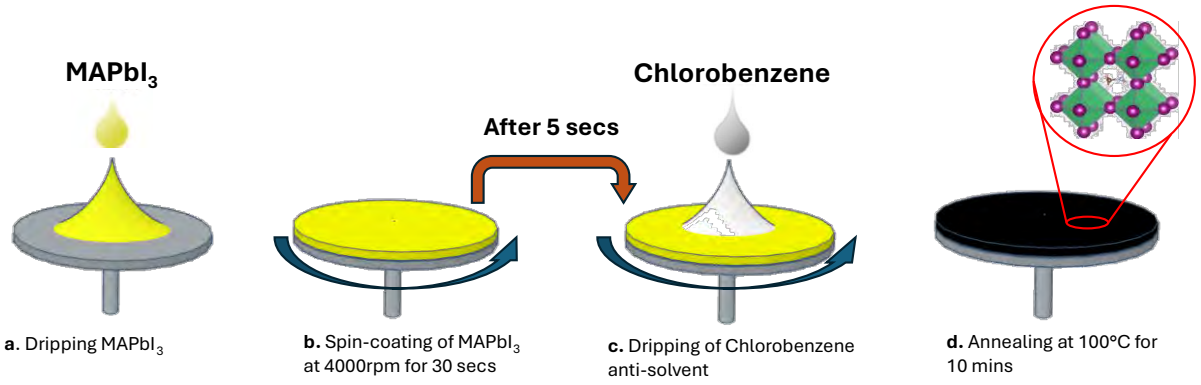

***Figure 4.11**: Deposition process of $MAPbI_3$*

When the anti-solvent is dispensed the solubility of the solution drops rapidly, so localized supersaturated nuclei are formed, and fast crystallization of the perovskite film is achieved during the spin-coating process. The rapid and dense nucleation of the perovskite results in uniform and pinhole-free films [106]. During the annealing step, the solvent (DMF) and the anti-solvent (chlorobenzene) are evaporated. The reaction between the precursors (MAI and PbI_2) and the formation of the perovskite, takes place after the release of the DMF molecules during the annealing [107]**.**

The crystal structure of $MAPbI_3$ perovskite was characterized by X-ray diffraction (XRD). The measured XRD spectrum is depicted in **Figure 4.12-left**. The pattern indicates well defined peaks at 2θ with 13.74, 19.62, 23.10, 24.12, 28.07, 35.51, 32.61, 34.60, 40.60, 42.83, 49.89,

corresponding to (110), (112), (211), (202), (220), (222), (310), (312), (224), (314) and (404) planes of the $MAPbI_3$ tetragonal phase, correspondingly, which is in good agreement with other works in the literature [108]. The very weak intensity peak with $2\theta = 12.28$ corresponds to the 001 plane of the PbI_2 [109]. The SEM image of the $MAPbI_3$ film is depicted in **Figure 4.12-right**, where its polycrystalline nature is apparent, with the crystallites' diameter being estimated between 100 and 250 nm in diameter.

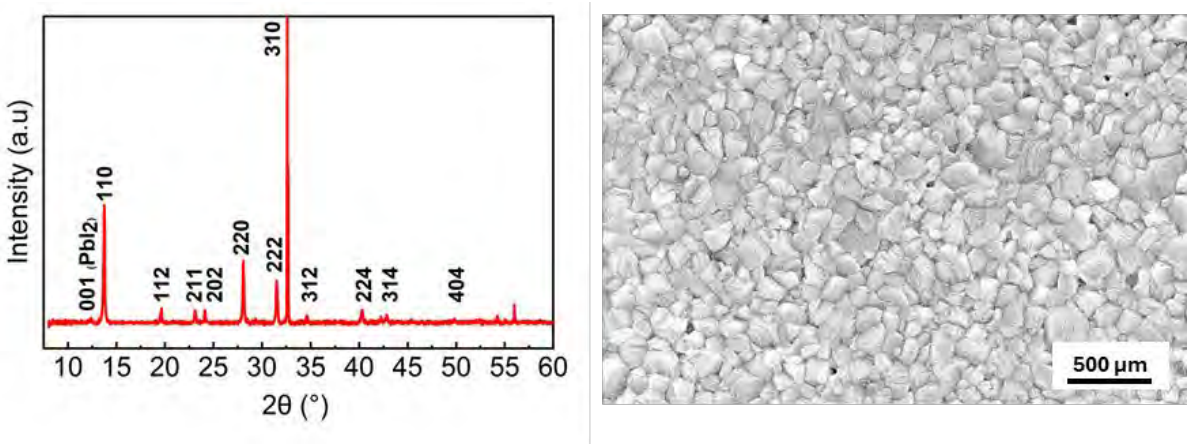

Figure 4.12: (left) *XRD spectrum of $MAPbI_3$ and assignment of the corresponding Miller indices.* ***(right)*** *SEM image of the $MAPbI_3$ film. Crystallites' diameter is estimated between 100 and 250 nm in diameter.*

4.5 Dielectrics Characterization

The leakage current of the AlO_x dielectric layers deposited by ALD and Sol-Gel method was measured by I-V measurements on $Si/AlO_x/Cr$ capacitors of various electrode sizes, i.e. 100µm x 100µm, 250µm x 250µm and 500µm x 500µm. A voltage bias (V_{app}) was applied between the top Cr electrode and the silicon substrate as illustrated in **Figure 4.13-left**.

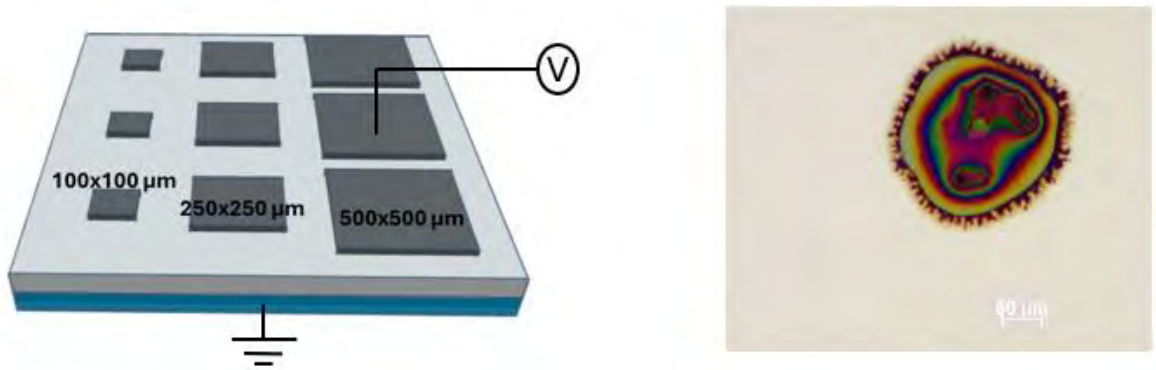

Figure 4.13: (left) *Capacitors measurements setup. The bias is applied among the substrate and the Cr contact.* ***(right)*** *characteristic crater-like spot on the Cr contact, caused due to dielectric discharge.*

In **Figure 4.14**, the current density is plotted in function with the applied electric field (E = V_{app}/d), where d is the thickness of the dielectric layer, measured by the spectroscopic reflectometer technique, $d_{Sol\text{-}Gel}$ = 18.71nm and d_{ALD} = 23.09 nm. The dielectric breakdown can be observed on those plots, by the rapid increase in the current density of the J-E curves. For the AlO_x Sol-Gel film, the dielectric breakdown was successful for all electrode sizes, while in the case of ALD-AlO_x, the breakdown did not occur for the big electrode (500x500μm) even at 13 MV/cm, or 30 V applied bias. **Figure 4.13-right** shows an image, taken with an optical microscope, of a characteristic breakdown spot on the Cr electrode, with a crater-like form and peripheral dendritic structures indicating the dielectric discharge and the successful breakdown of the dielectric film, as also reported in a previous work [110].

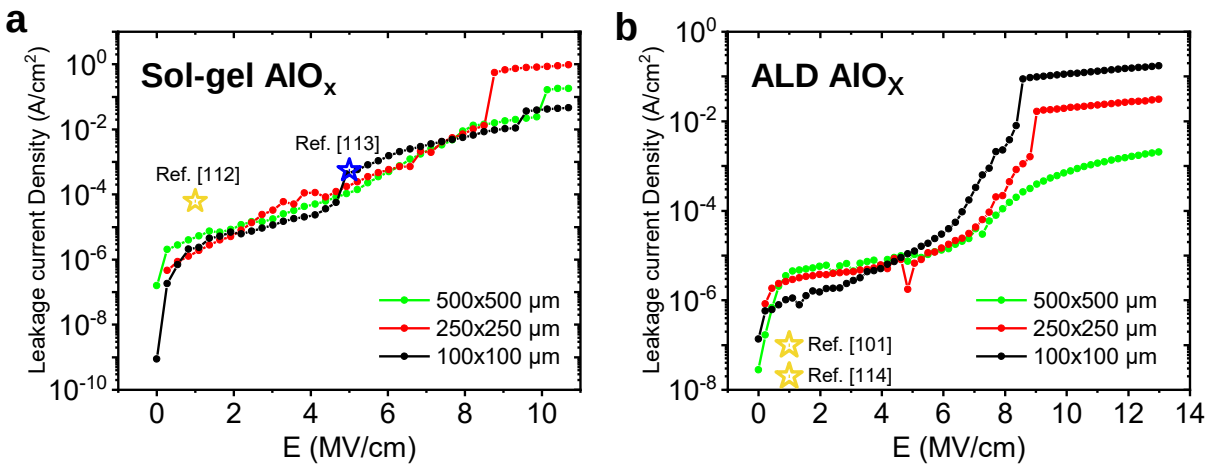

***Figure 4.14**: **Dielectric breakdown measurements on capacitors with**: **a)** Sol-Gel AlOx dielectric layer and **b)** ALD-AlOx dielectric layer. Each color corresponds to a different contact surface area. Star symbols correspond to literature values.*

It is worth mentioning that there is no clear dependence of the leakage current density with the electrode area size. This indicates that the dielectric films are homogeneous and free of pinholes, which are common defects of a dielectric, causing short circuits between the two electrodes [111]. If pinholes existed the leakage current would flow through the pinhole and would have the same values for all the electrode area dimensions, while the leakage current density would be different (as it is divided by the different electrode area), which is not the case here.

The leakage current behavior of AlO_x Sol-Gel seems to be in excellent agreement with similar works in the literature, while in the case of AlO_x ALD, it exhibits higher leakage currents compared to reported values. Specifically, for the AlOx Sol-Gel dielectric, the leakage current density was measured 2.36 μA/cm² at 1 MV/cm and 0.426 mA/cm² at 5 MV/cm. These values

are consistent and even lower compared to the findings of Avis et al. [112], who reported 63 μA/cm², and Wei et al. [113], who reported 0.553 mA/cm² at 1 MV/cm² and 5 MV/cm², respectively. In the case of AlOx ALD, the current density was measured at 1.12 μA/cm² at 1 MV/cm, which is higher by one or two orders of magnitude compared to the values reported in the literature, such as ~0.1 μA/cm² by Groner et al. [101] and ~0.02 μA/cm² by Oh et al. [114] (literature values are also presented in **Figure 4.13**). This indicates the relatively poor quality of the ALD-AlOx dielectric film and could, probably, be attributed to the big amount of unreacted precursor, during the deposition. Further experimentation and optimization of the deposition should be done to reduce the amount of defects in the film and minimize the leakage current.

4.6 Synaptic-Transistor Devices Characterization

4.6.1 Substrate-as-gate transistor electrical characterization

The memristive character of the perovskite can be studied by applying a voltage bias along the drain-source electrodes (V_{DS}). A voltage sweep from 20V to -20V and then back to 20V at a scan rate of 2V/s is applied, and a hysteresis loop is formed as depicted in **Figure 4.15a**. Starting from 20V towards 0V a lower current amplitude is measured, while with a small negative bias, a higher current is measured from 0V to -20V. In the backward sweep, from -20 V to 0 V, the current amplitude is lower, and finally, a higher current output is measured from 0V to 20V it increases.

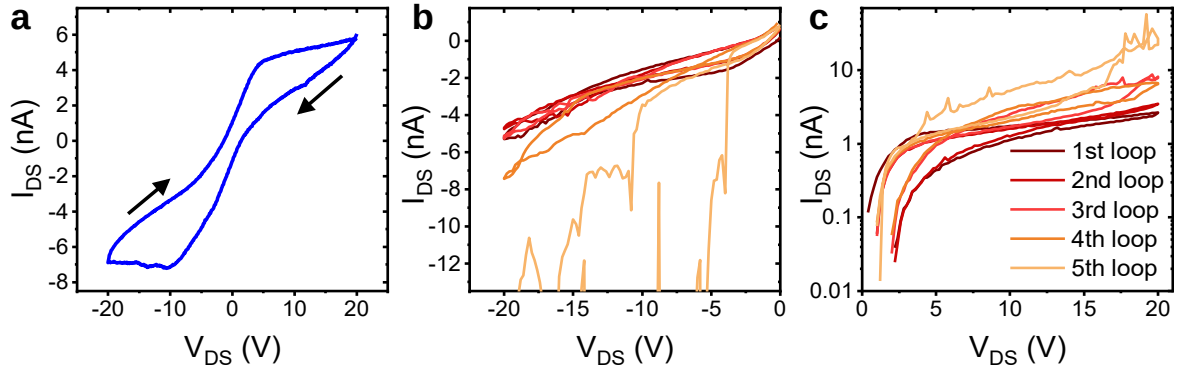

Figure 4.15**: **Memristive behavior of the 1mm x 500μm channel a)** I-V characteristic measurement of the channel with scanning rate 2V/s. Arrows indicate the voltage sweep direction. **b)** evolution of the resistance state of the channel after 5 consecutive negative voltage loops. **c)** Evolution of the resistance state of the channel after 5 consecutive positive voltage loops. The legend of **(c)** also corresponds to **(b).

By applying consecutive positive or negative loops, with the same bias, an evolution in the resistance state is observed, as a higher current is measured after each loop, as shown in **Figure 4.15b-c**. This is one of the central properties of memristors [115]. The plot of **Figure 4.15b** has been magnified for clearer visualization of the data, as in the 5th loop the current increases rapidly due to the breakdown of the perovskite in the channel. The plot without magnification of the data is depicted in Appendix **Figure A6. 4**.

The transistor transfer characteristics can be extracted when the gate bias is also applied. Modulation of the drain-source current is observed when the gate voltage is increased negatively while there is no significant effect in the I_{DS} for positive gate voltages, as shown in **Figure 4.16a**. This indicates that the channel mainly consists of positive carriers (holes), which are attracted from the bulk semiconductor by the positive gate voltage and accumulated on the perovskite/dielectric interface. For constant drain-source voltage, there is increasing I_{DS} as positive gate-source voltage increases (**Figure 4.16b**).

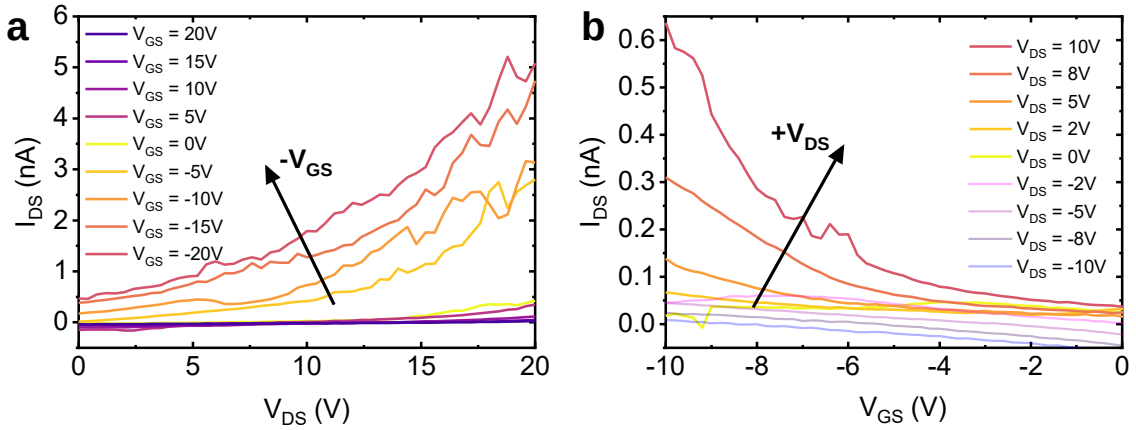

Figure 4.16: a) *Output characteristic with drain-source voltage sweep and constant gate voltage. The arrow indicates the modulation of the current when the negative gate voltage increases.* ***b)*** *output characteristic with gate-source voltage sweeps and constant drain-source voltage. The arrow indicates the modulation of the current when the positive drain-source voltage increases*

To investigate the synaptic characteristics of the device, gate voltage pulses (V_{GS}) and constant drain-source voltage (V_{DS}), are applied as shown in **Figure 4.17**. The changes in the output post-synaptic current are measured with the application of a continuous V_{DS} (reading voltage).

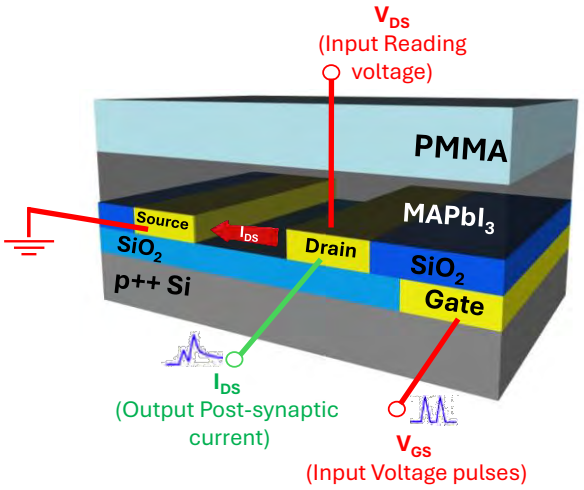

Figure 4.17: *Schematic representation of the measurement setup for the substrate-as-gate transistor. Constant gate pulses, V_{GS} (writing voltage) and continuous drain-source voltage, V_{DS} (reading voltage), are applied. The I_{DS} post-synaptic current is measured as output.*

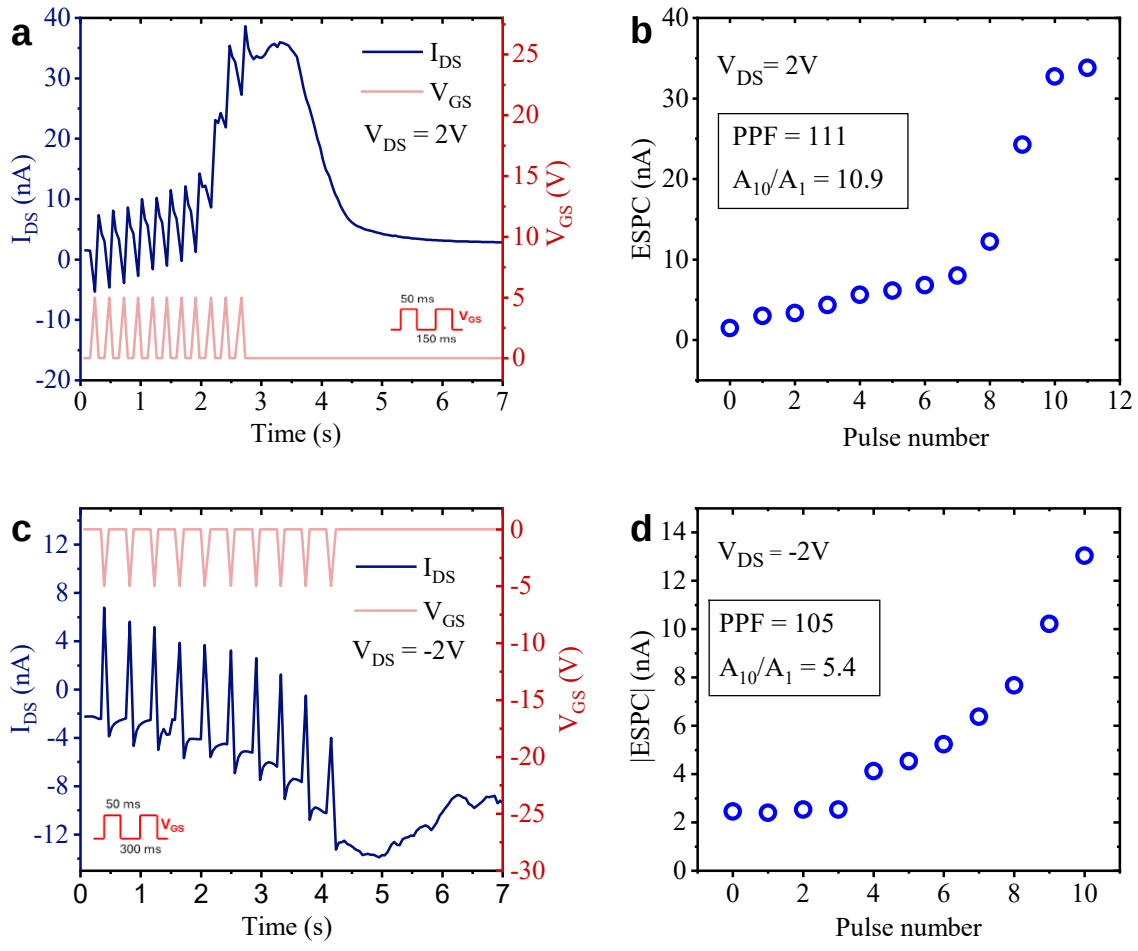

Figure 4.18: Measurements on 10 µm x 1 µm channel of substrate-as-gate transistor*. **a)** Input constant voltage pulses of 5V, 50ms duration, and 150 ms time interval (red curve) and post-synaptic current measured with V_{DS} = 2V (blue curve). **b)** Post-synaptic current as a function of pulse number, corresponding to the data of **(a)**. PPF = 111 and A_{10}/A_1 = 10.9 were calculated. **c)** Input: constant voltage pulses of -5V, 50ms duration, and 300 ms time interval (red curve) and post-synaptic current*

measured with V_{DS} = -2V (blue curve). ***d)*** *Post-synaptic current as a function of pulse number, corresponding to the data of* ***(c)****. PPF = 105 and A_{10}/A_1 = 5.4 were calculated.*

Eleven consecutive gate voltage pulses of 5V and 50 ms in duration and 150 ms time interval (duration between two pulses) and a continuous reading drain-source voltage of 2V are applied, as shown in **Figure 4.18a**. During the gate pulse, the drain-source current decreases due to the screening effect on the gate bias, caused by the ion migration. After the gate pulse, the current increases and then decays as the ions diffuse back. [38]. The measured I_{DS} current is also called excitatory postsynaptic current (EPSC). To study the behavior of the EPSC, the value of the current before each gate pulse (at the end of the current decay) is plotted in function of the gate pulse number. As shown in **Figure 4.18b,** the current increases gradually after each gate pulse, with a rapid increase (almost double its value) after the eighth pulse from 12.2 nA to 24.2 nA. The reason behind this rapid increase in EPSC is not clear. It could be related to a gradual accumulation of ions near the gate region, after the consecutive gate pulses, affecting significantly the conductance of the channel, especially after the eight pulse. The PPF factor is calculated to 111 and by calculating the gain, meaning the ratio of the current value after the tenth pulse to the current after the first pulse (A_{10}/A_1), the current increases 10.9 times. This behavior demonstrates the ability of gate pulses to tune the conductance state of the channel.

As **Figure 4.18c,d** shows that when the duration between gate pulses doubles to 300 ms, the PPF factor decreases by 5.4% to the value of 105, while the gain (A_{10}/A_1) decreases by 50.4%, to the value of 5.4, compared to the previous case. The decreasing of PPF factor with increasing pulse interval is consistent with the behavior of a typical biological synapse [66]. The gate pulse induces the migration of the iodine vacancies, V_I, in the channel thus creating conductive paths at the dielectric-perovskite interface [105], lowering the resistance of the channel. If the second pulse is applied rapidly before the recovery time (or the recombination) of the vacancy or the ions, it can accelerate the V_I migration [58]. Thus, a smaller time interval, between two pulses, results in a higher PPF factor.

The effect of the pre-poling was also studied. The device is pre-polled with a drain-source voltage of 7 V for 9.5 seconds (green line in **Figure 4.19a**). Directly then, ten consecutive gate pulses of 5V, 50ms duration, and 150 ms time interval are applied and a continuous V_{DS} = 2V, as shown in **Figure 4.19**. From the plot of the post-synaptic current in the function of the pulse number, it can be seen that the PPF factor increases significantly to the value of 197, while the ratio A_{10}/A_1, with a value of 4.72, decreases compared to the previous cases.

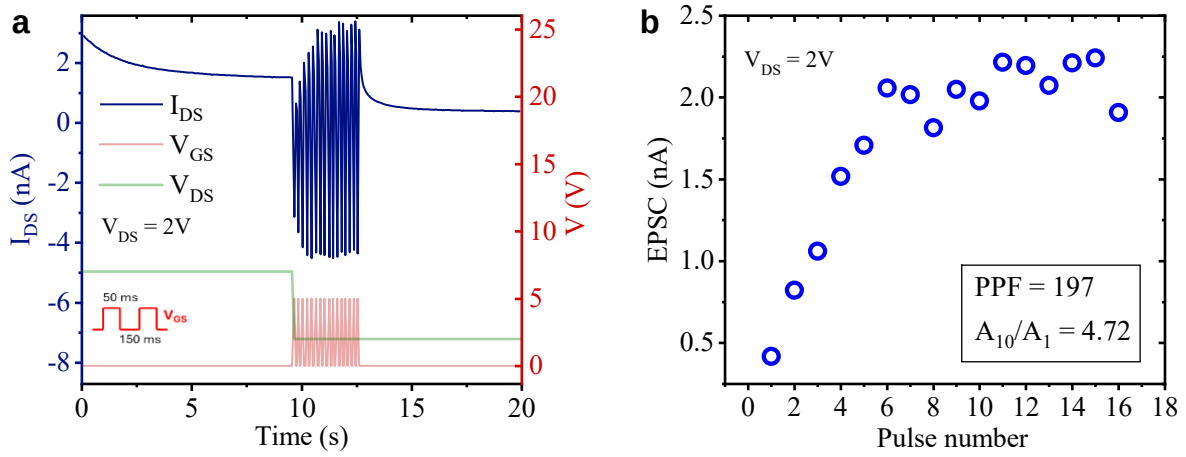

Figure 4.19: Measurement on 1 mm x 10 µm channel of substrate-as-gate transistor. a) *Input: constant voltage pulses of -5V, 50ms duration, and 300 ms time interval (red curve), continuous V_{DS} = 7V (green curve) is applied before the pulses to pre-pole the channel. Post-synaptic current is measured with V_{DS} = -2V (blue curve).* ***b)*** *Post-synaptic current as a function of pulse number. PPF = 197 and A_{10}/A_1 = 4.72 were calculated.*

The pre-poling sets the device to the high resistance state (HRS) by causing the ions (mainly iodide anions) to migrate toward the source contact modifying the effective Schottky barrier, as reported by the reference [36]. As shown in previous measurements consecutive gate pulses update the conductance of the device to higher conductance states (or lower resistance states), the first pulses seem to cause a more pronounced conductance change, as the initial state is the HRS. The update of the conductance states is prominent only for the first six pulses, staying relatively constant after the sixth pulse. This could be attributed to the fact that only a certain amount of iodide/iodide vacancies can be attracted, by the gate pulses, on the perovskite/dielectric interface. It seems that after six pulses there has been a high concentration of ions/vacancies on the interface that repel each other to such a degree that cancels out the drift of more ions to the interface, stabilizing the distribution of the ions on the interface and the conductance state of the channel as well. At the same time, the gate electric field is also screened to a high degree, by the electric field of the accumulated ions, eliminating the effect of the gate to attract more ions.

Capacitive response

While the previously presented measurements show an update in the current after each gate pulse, which could be attributed to the actual change in the channel conductance, there are cases where the measured current is in the opposite sign compared to the V_{DS} reading voltage, which is not reasonable, as shown in **Figure 4.20,** where negative gate pulses and a positive continuous V_{DS} reading voltage are applied. The reading post-synaptic current has negative

values after the third pulse, as shown in **Figure 4.20b**. This could indicate that the current originates from a capacitive displacement current as mobile ions are pushed away or are attracted to the source and drain electrodes, rather than from a change in the channel conductance. This opposite sign current is something that Xiao et al. have also reported on their $MAPbI_3$ memristor [38]. Furthermore, in the substrate-as-gate transistor configuration, the whole substrate acts as a gate electrode, and a capacitor is formed with the substrate as the one electrode, the contact pads (the gold squares on the SiO_2 layer, where the probes of the drain and source voltage are placed), as the top electrode, and the SiO_2 layer between them, as the dielectric layer. This capacitor can also charge/discharge, by the application of the gate pulses, creating a capacitive current contributing to the measured source-drain current.

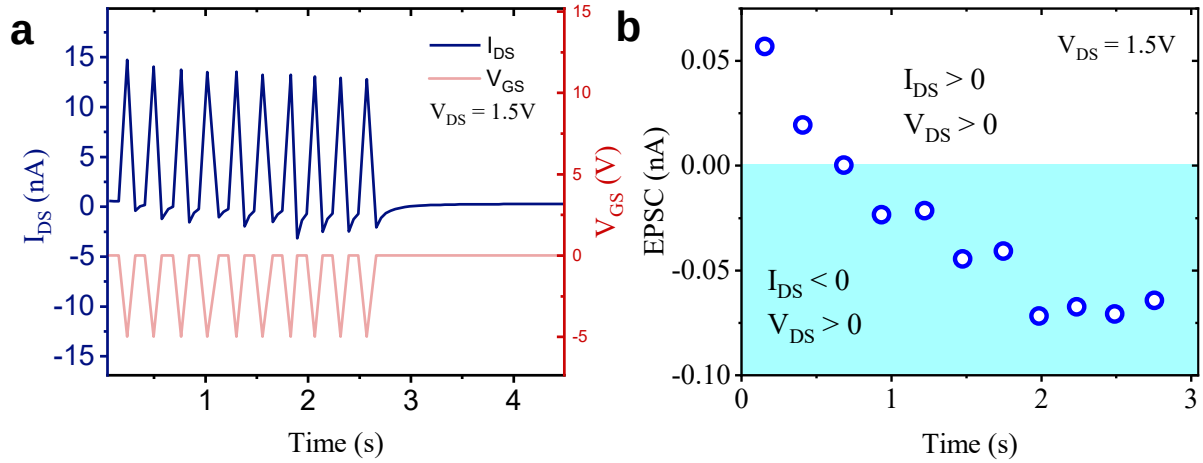

Figure 4.20: Capacitive response. Measurement on 100 nm x 50 nm channel. a) *Input: constant voltage pulses of -5V, 50ms duration, and 150 ms time interval (red curve) and post-synaptic current measured with* V_{DS} *= 1.5V (blue curve).* ***b)*** *Post-synaptic current as a function of pulse number. Capacitive response due to ion migration as negative EPSC is measured despite the positive* V_{DS} *= 1.5V reading voltage. Blue shaded area corresponds to data where* I_{DS} *has an opposite sign than* V_{DS} *(*I_{DS} *< 0 and* V_{DS} *> 0).*

To address this issue, a new transistor configuration needs to be fabricated, where the gate electrode should be distinct and have a separate contact pad rather than the whole substrate as in the previous case. Thus, the so-called, bottom-gate transistor is fabricated as previously discussed in the section **4.2** .

4.6.2 Bottom-gate transistor electrical characterization

In the bottom-gate transistor configuration, a distinct gate electrode is patterned on the Si/SiO_2 substrate, a dielectric layer is deposited on the top and finally, the drain and source electrodes are patterned on the dielectric, as shown in **Figure 4.21**.

The dielectric layer chosen for this device is the aluminum oxide (AlO_x) dielectric, which has been synthesized by two different methods, the Sol-Gel method and the Atomic Layer Deposition (ALD) method. In this section, the electrical measurements of the transistor with the ALD dielectric are first presented, and then the device with the Sol-Gel AlO_x dielectric. The measurement setup is also illustrated in **Figure 4.21**, where input gate pulses are applied by one channel and a continuous drain-source voltage is applied by a second channel. The post-synaptic current is measured by the change in the current of the second channel.

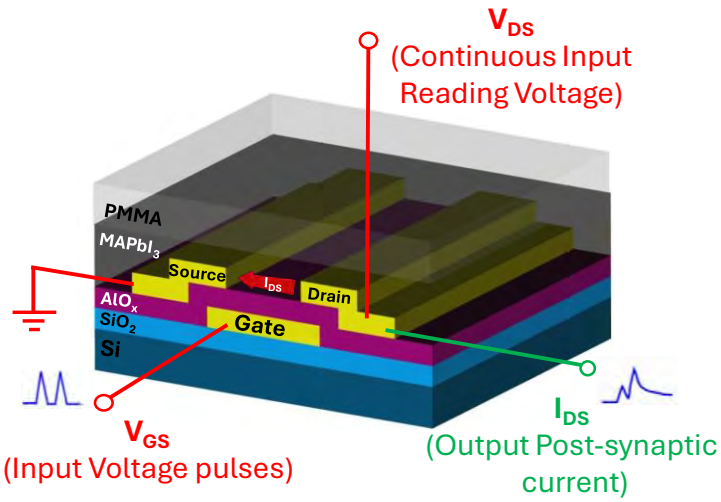

***Figure 4.21**: Schematic representation of the measurement setup for the bottom -gate transistor. Constant gate pulses, V_{GS} (writing voltage) and continuous drain-source voltage, V_{DS} (reading voltage), are applied. The I_{DS} post-synaptic current is measured as output.*

4.6.2.1 ALD - AlO_x gate dielectric

A gradual change in the channel conductance is observed for the device with the ALD-AlO_x dielectric layer as depicted in **Figure 4.22a,b**. Ten consecutive gate pulses are applied of -5V, 50ms duration, and 150ms time interval, and the synaptic current increases after each pulse. The PPF factor is calculated as 112 and the ratio A_{10}/A_1 is 1.40.

For a bigger pulse duration (200ms), as shown in **Figure 4.22c,d** the PPF factor increases 19% more, at the value of 133, and the ratio A_{10}/A_1 increases by 22%, at the value of 1.71, compared to the previous case. The increase of those terms with increasing pre-synaptic pulse duration is consistent with the biological artificial synapse function, as the mobile ions in the perovskite are stimulated for a longer duration by the gate pulse, leading to more significant accelerated ion migration [62].

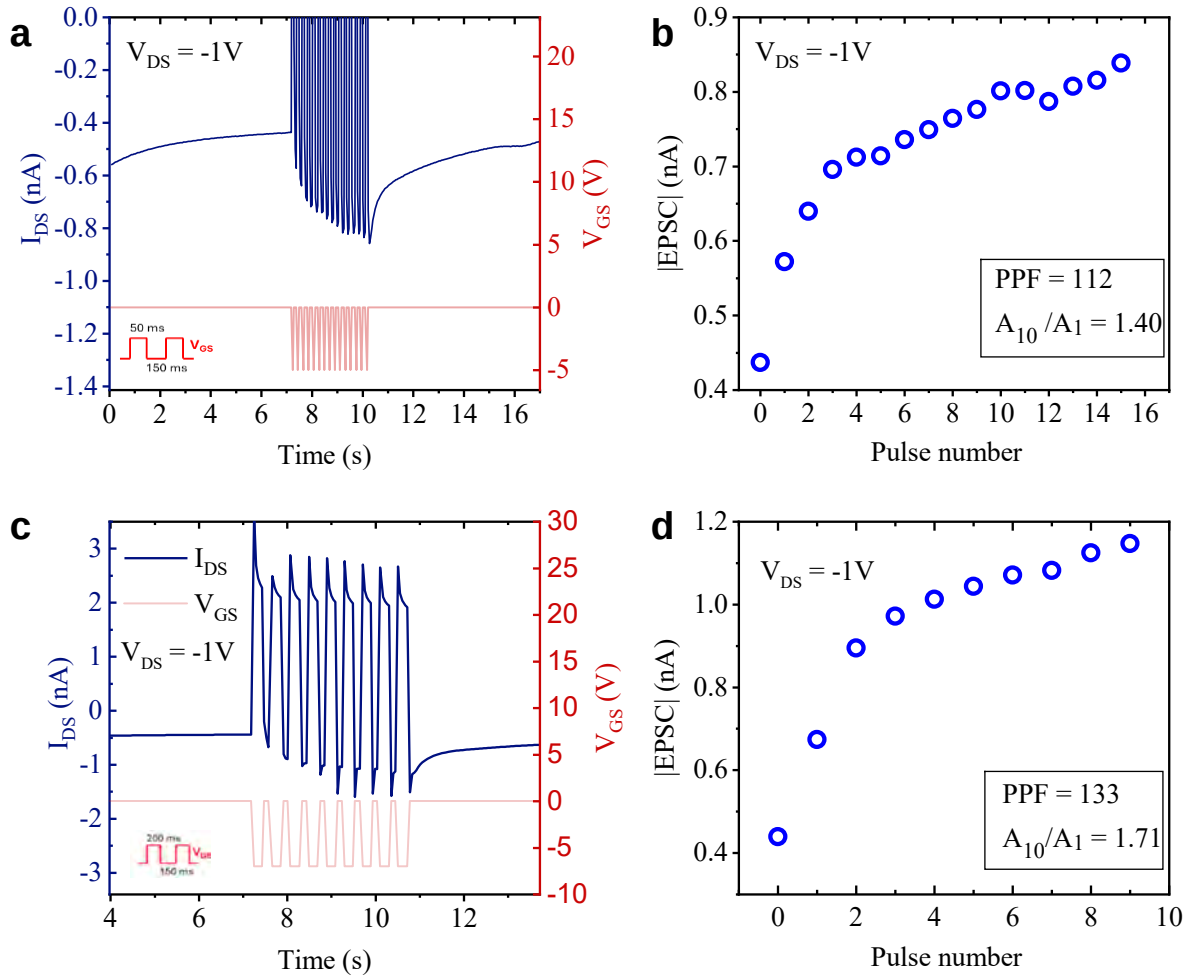

Figure 4.22: Measurements on 100 nm x 50 nm channel of bottom-gate transistor with ALD AlOx gate dielectric a) *Input: constant voltage pulses of -5V, 50ms duration, and 150 ms time interval (red curve) and post-synaptic current measured with V_{DS} = -1V (blue curve).* ***b)*** *Post-synaptic current as a function of pulse number, corresponding to the data of* ***(b)****. PPF = 112 and A_{10}/A_1 = 1.40 were calculated.* ***c)*** *Input: constant voltage pulses of -7V, 200ms duration, and 150 ms time interval (red curve) and post-synaptic current measured with V_{DS} = -1V (blue curve).* ***d)*** *Post-synaptic current as a function of pulse number, corresponding to the data of* ***(c)****. PPF = 133 and A_{10}/A_1 = 1.71 were calculated.*

4.6.2.2 Sol-Gel AlO_x gate dielectric

The device with the Sol-Gel AlOx dielectric also demonstrated synaptic functions but it showed the lowest performance. The PPF factor and A_{10}/A_1 ratio were calculated at 104 and 1.15 respectively, as shown in **Figure 4.23a,b**, where fifteen gate pulses were applied of -2V, 100 ms duration, and 150 ms time interval and a V_{DS} = -0.5V reading voltage. The PPF and the A_{10}/A_1 ratio remained almost the same even when -10V voltage pulses were applied as shown in **Figure 4.23c,d**.

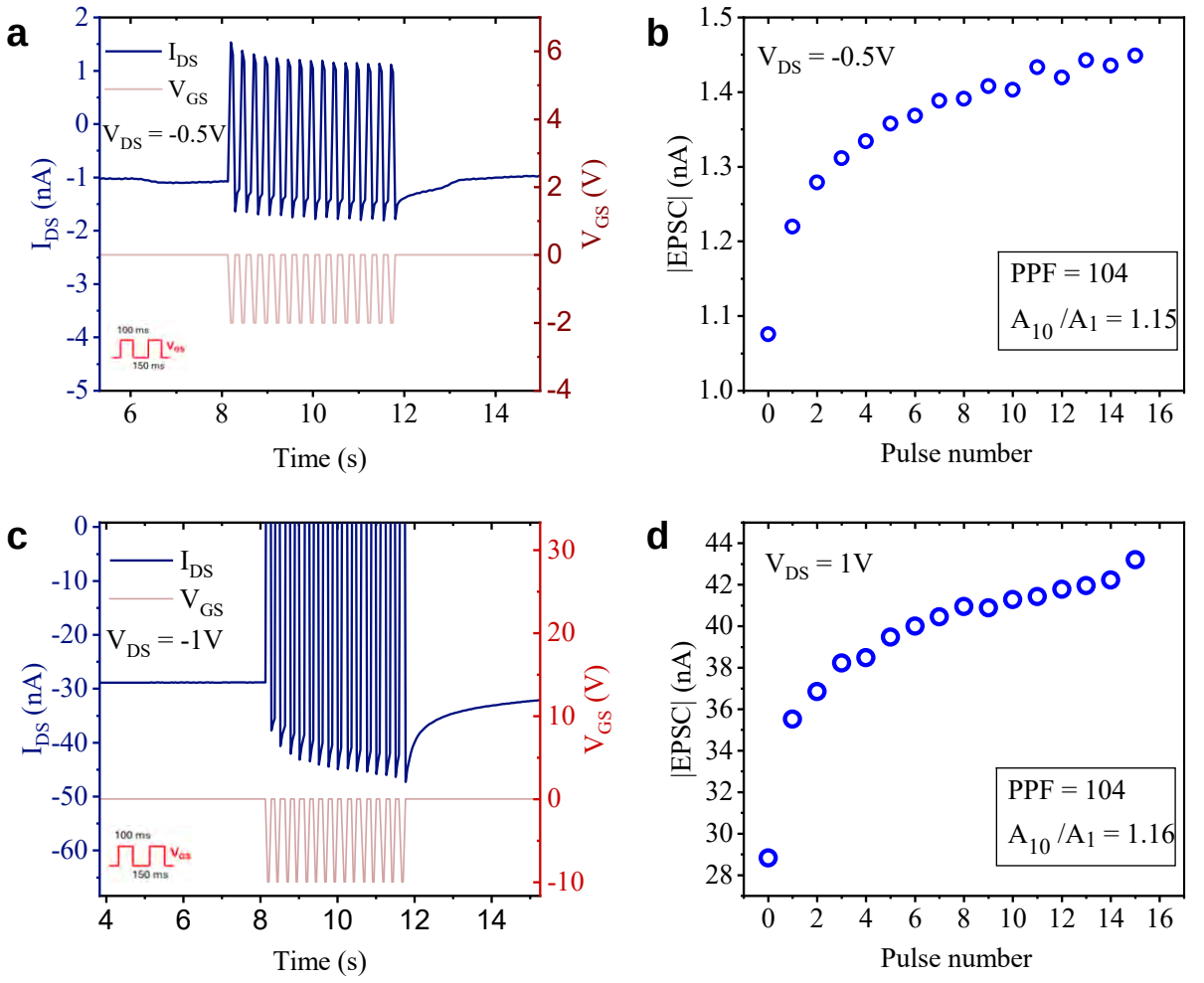

***Figure 4.23**: **Measurement on 100 nm x 50 nm channel of bottom-gate transistor with Sol-Gel AlOx gate dielectric. a)** Input: constant voltage pulses of -2V, 100ms duration, and 150 ms time interval (red curve) and post-synaptic current measured with V_{DS} = -0.5V (blue curve). **b)** Post-synaptic current as a function of pulse number, corresponding to the data of **(a)**. PPF = 104 and A_{10}/A_1 = 1.15 were calculated. **c)** Input: constant voltage pulses of -10V, 100ms duration, and 150 ms time interval (red curve) and post-synaptic current measured with V_{DS} = -0.5V (blue curve). **d)** Post-synaptic current as a function of pulse number, corresponding to the data of **(c)**. PPF = 104 and A_{10}/A_1 = 1.16 were calculated.*

4.6.3 Electrical measurements under continuous light–illumination

The response of the devices under both electrical stimulation and light illumination has also been studied. It is reported that the migration of the iodine vacancy is further accelerated under light illumination and is considered to be responsible for further modification of the synaptic behavior, yielding interesting results [32]. There have been multiple works in the literature with optoelectronic perovskite synaptic transistors, where a light source stimulates the device by light pulses or continuous illumination [36], [86], [41], [116], [33], [32].

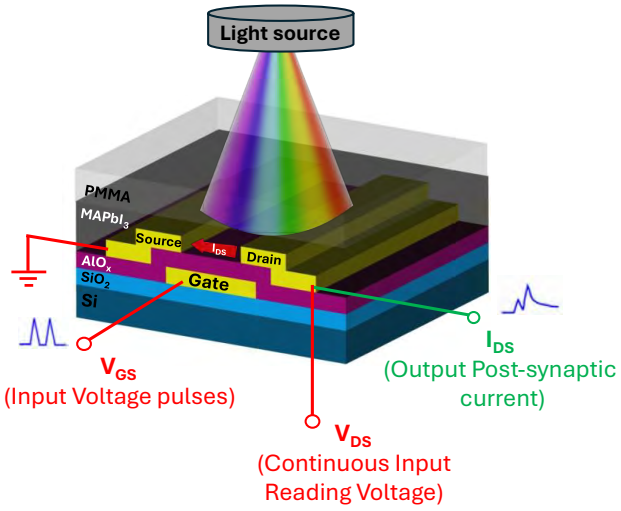

***Figure 4.24**: Schematic representation of the electrical measurements setup, under light illumination. The device is continuously illuminated by white light. Pre-synaptic gate voltage pulses are applied by the gate-source electrodes (V_{GS}) and a continuous drain-source voltage (V_{DS}) to read the output post-synaptic current of the channel I_{DS}.*

4.6.3.1 Bottom gate – transistor with ALD - AlO_x gate dielectric

The effect of light illumination in combination with the applied gate voltage, on the bottom-gate transistor with the ALD-AlO_x dielectric, was investigated. The measurements setup under those conditions is illustrated in **Figure 4.24**. **Figure 4.25a** shows a transient measurement where the device was continuously illuminated by white light of 0.8 mW/cm^2. A constant drain-source voltage (V_{DS}) of 1V was applied during the measurement to tread the current of the channel. Initially, without any gate voltage, the current remained constant. After 7 seconds, a gate bias of -5V was applied for 9 seconds, resulting in an increasing current, from 3.1 nA to 19.2 nA, or a 520% increase. When the gate bias was subsequently changed to +5V, the current after decaying remained at a constant value.

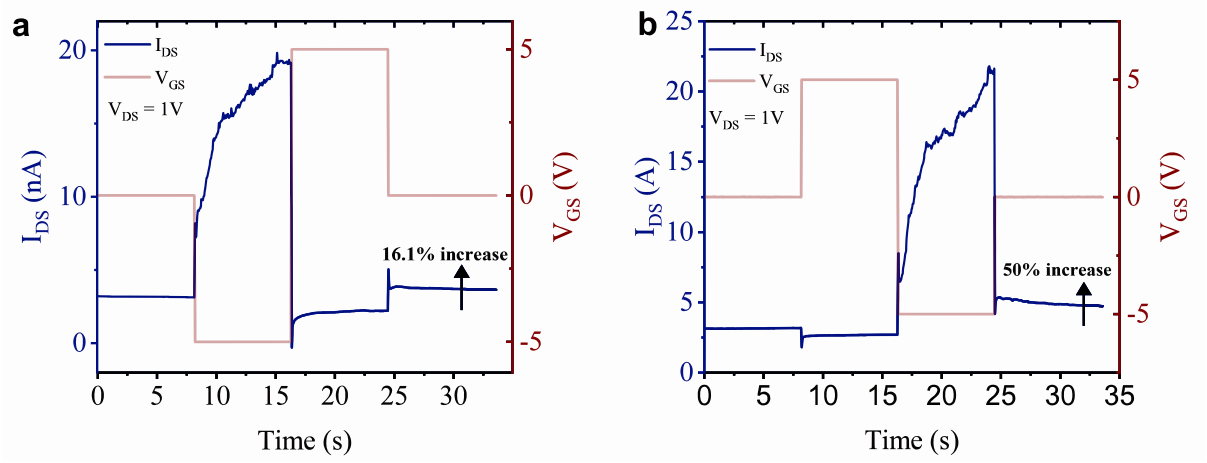

***Figure 4.25: Measurement on 100 nm x 50 nm channel under 0.8 mW/cm^2 light illumination of the bottom-gate transistor with ALD AlOx gate dielectric.** **a)** Input: V_{GS} = -5V for 9 sec and then V_{GS} =*

5V for 9 sec (red curve). Output: Post-synaptic current is measured with V_{DS} =1V reading voltage. After the long-gate pulses, the current is increased by 16.1% compared to the base current before the pulses. ***b)*** *Input: V_{GS} = +5V for 9 sec and then V_{GS} = -5V for 9 sec (red curve). Output: Post-synaptic current is measured with V_{DS} =1V reading voltage. After the long-gate pulses, the current is increased 50% higher compared to the base current before the pulses.*

The same measurement was taken, but with the positive gate bias applied first, followed by the negative gate bias, as shown in **Figure 4.25b**. The results were similar, this time with a 693% increase in the current at the end of the negative gate bias, demonstrating clearly, the effect of the negative gate voltage in increasing the channel conductance when the device is illuminated.

It is also noteworthy that the current stays at a higher level after the end of the gate stimulations (increased by 16.1% for the first measurement **Figure 4.25**a and 50.5% for the second one, **Figure 4.25b**), clearly demonstrating the LTP mechanism.

The reason for the prominent potentiation of the current only by negative gate pulse could be attributed to the increased concentration of positive charged iodine vacancies (V_I) in the channel, which act as conductive paths lowering significantly the resistance of the channel [36], [105]. Under light illumination ion migration is further accelerated [32]. Positive gate bias on the other side repels the positive V_I resulting in a decay of the post-synaptic current due to the diffusion of ions out of the channel.

As the effect of the negative gate bias under light illumination gives rise to the modulation of the conductance states of the device the application of short negative gate pulses is studied with the device being illuminated at the same time.

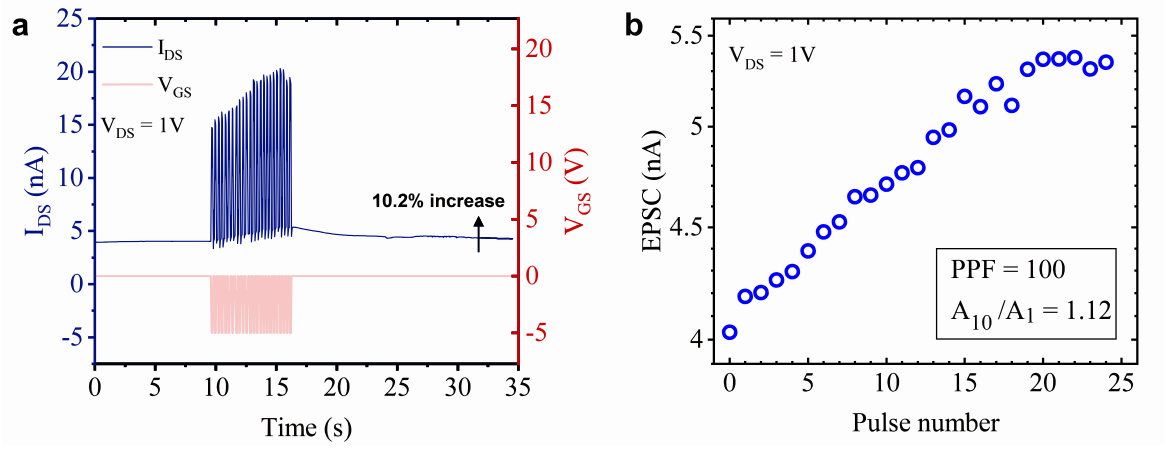

Figure 4.26**: **Measurement on 100 nm x 50 nm channel of bottom-gate transistor with ALD AlOx gate dielectric.. a)** Input: constant voltage pulses of -5V, 50ms duration, and 150 ms time interval (red curve). Output: post-synaptic current measured with V_{DS} = 1V (blue curve).* ***b) *Post-synaptic current as a function of pulse number. PPF = 100 and A_{10}/A_1 = 1.12 were calculated. The base current increases 10.2% compared to the base current before the pulses.*

When gate pulses are applied (-5V, 50 ms duration and 150 ms time interval), under 0.8 mW/cm^2 light intensity, **Figure 4.26**, the PPF factor was calculated as 101, while the A_{10}/A_1 ratio as 1.12. The current of the last pulse is increased 1.28 times higher compared to the first pulse' current. Interestingly, the conductance states are updated linearly, even after multiple pulses, while the base current stays 10.2% higher compared to the current before the pulses, even after 10 s, as shown in **Figure 4.26a**, demonstrating the LTP mechanism.

Except for the LTP mechanism, the LTD mechanism was also demonstrated, as shown in Figure 4.27. Under 8 mW/cm^2 continuous light intensity, by applying 34 consecutive negative gate pulses of -5V, 100 ms, an extended synaptic current modulation is achieved (leading to 1.36 times higher current after the last negative pulse). By the application of positive gate pulses of 5V, 100 ms the current is depressed (1.37 times lower current after the last positive pulse) as shown in **Figure 4.27b**. The potentiation and the depression of the conductance states is a central function of the artificial synapses, connected to learning and forgetting mechanisms, respectively, as the synaptic weight between two neurons can be enhanced or suppressed.

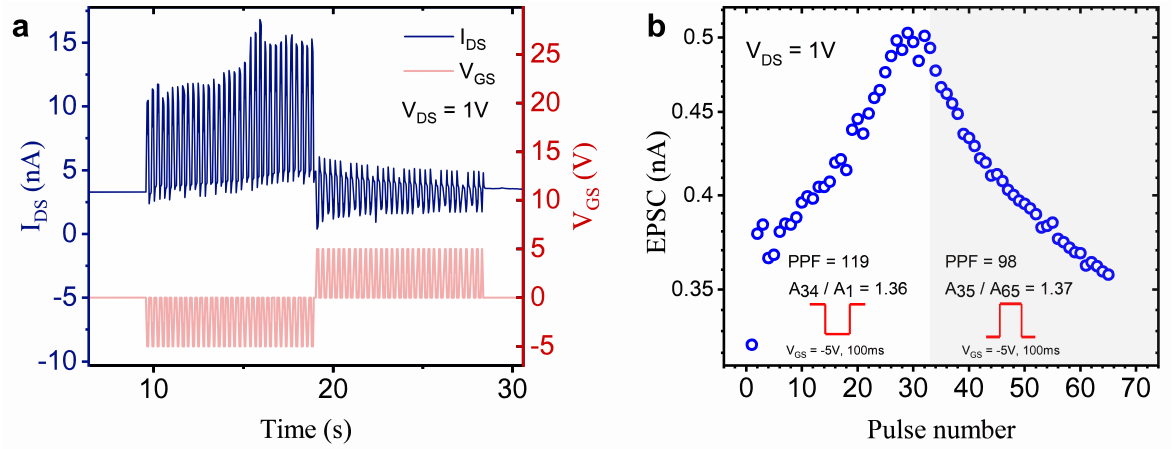

Figure 4.27: Demonstration of the long-term potentiation (LTP) and long-term depression (LTD) mechanism. a) *Input: 34 negative gate pulses of -5V, 100ms for the LTP, and 34 positive gate pulses of 5V, 100ms for the LTD (red curve). Output: post-synaptic current (blue curve).* ***b)*** *Post-synaptic current, measured with VDS = 1V, in the function of pulse number The current increases for the first negative gate pulses, indicating the LTP mechanism, with the current being 1.36 times higher on the 34th pulse. The current decreases when positive gate pulses are applied.*

4.6.3.2 Substrate-as-gate transistor

For the substrate-as-gate transistor, the continuous light illumination with an intensity of 80 mW/cm^2 enhances the PPF factor significantly, i.e. 55.9% more, as shown in **Figure 4.28**, compared to the first non-illuminated measure presented in the section **4.6.1** . The ratio A_{10}/A_1 is calculated at 6.19, decreased by -43.2%. Also, the conductance states show a relatively higher linear relation.

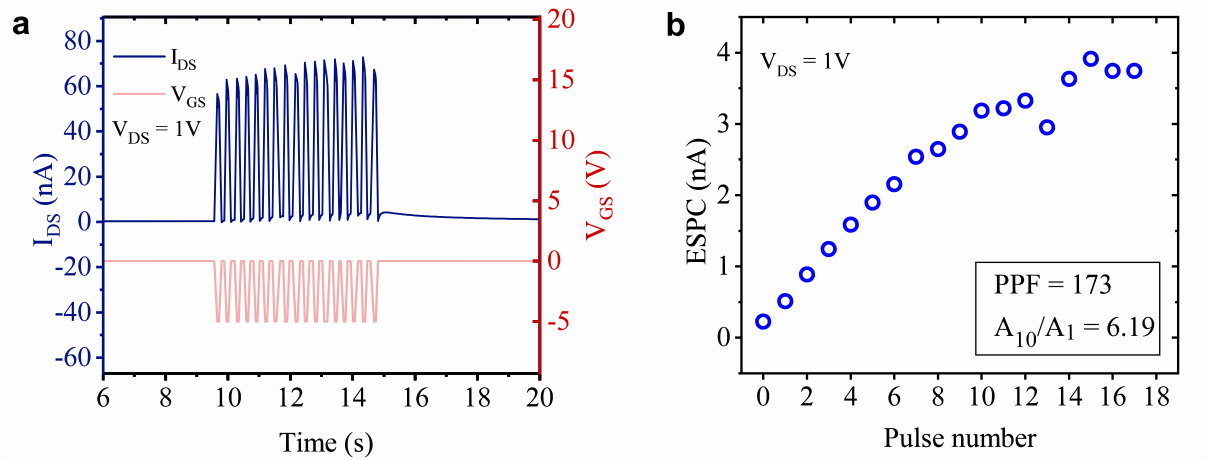

Figure 4.28: Measurement under 80mW/cm² light illumination of the 10μm x 500nm channel of substrate-as-gate transistor. a) *Input: constant voltage pulses of -5V, 50ms duration, and 150 ms time interval (red curve). Output: post-synaptic current measured with V_{DS} = 1V (blue curve).* ***b)*** *Post-synaptic current as a function of pulse number. PPF = 173 and A_{10}/A_1 = 6.19 were calculated.*

Light illumination seems to increase the PPF factor and decrease the ratio A_{10}/A_1. The measurement, with the device being illuminated and non-illuminated also confirms this, as shown in **Figure 4.29**. Consecutive gate pulses of -5V are applied on the bottom-gate transistor with AlO_x dielectric. After ten pulses the device begins to be illuminated. The initial post-synaptic current value, during illumination, starts at a higher level, due to the photogenerated current, meaning, the rapid creation of electron-hole pairs within picoseconds when photons with energy equal to or greater than the bandgap energy are absorbed [58], [109]. The PPF factor before illumination is 103 and during illumination, it increases by 7.8% at 111, while the ratio A_{10}/A_1 is 1.41 and decreases by -9.9% at 1.27, for the illuminated measurements. The suppression of the current ratio under light illumination is consistent with the work of Rogdakis et al. [36] and Zhu et al. [117].

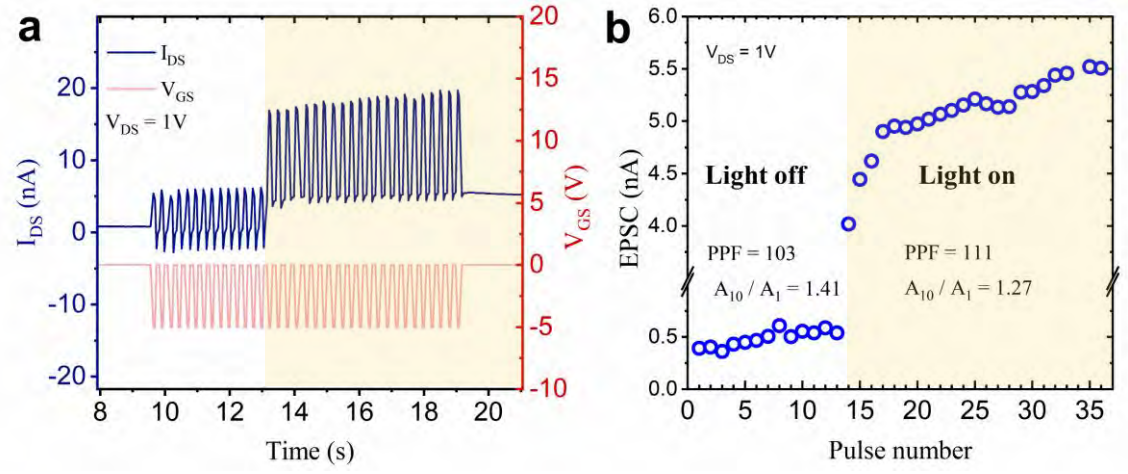

Figure 4.29: a) *Input: constant voltage pulses of -5V, 50ms duration, and 150 ms time interval (red curve). The sample is exposed to continuous light illumination with* ***6.9 mW/cm²*** *intensity, after the 14th*

gate pulse. Output: post-synaptic current measured with V_{DS} = 1V (blue curve). ***b)*** *Post-synaptic current as a function of pulse number. Without light illumination PPF = 103 and A_{10}/A_1 = 1.41 were calculated. Under light illumination, PPF increased to 111 and the ratio A_{10}/A_1 decreased to 1.27.*

4.6.4 Electrical measurements under light pulses

Instead of continuous light illumination, light pulses are also used to stimulate the channel conductance of the ALD-AlO_x bottom-gate transistor. Firstly, the effect of the gate voltage on the postsynaptic current is studied, while the device is illuminated by light pulses. Light pulses with 6.9 mW/cm^2 intensity, 100 ms duration and 50 ms time interval were applied. Without the application of the gate bias, no conductance modulation is observed, as shown in **Figure 4.30a**, in contrast, the post-synaptic current is decreased with a PPF factor of 99. When a continuous gate voltage of -5V is also applied during the measurements, the modulation of the postsynaptic current is achieved (PPF = 102), after each light pulse, as shown in **Figure 4.30a**. This suggests the light illumination effect in the device, without the electrical stimuli, by the gate electrode, may be not sufficient to cause the migration of iodine vacancies V_I and form a conductive path in the perovskite film [32].

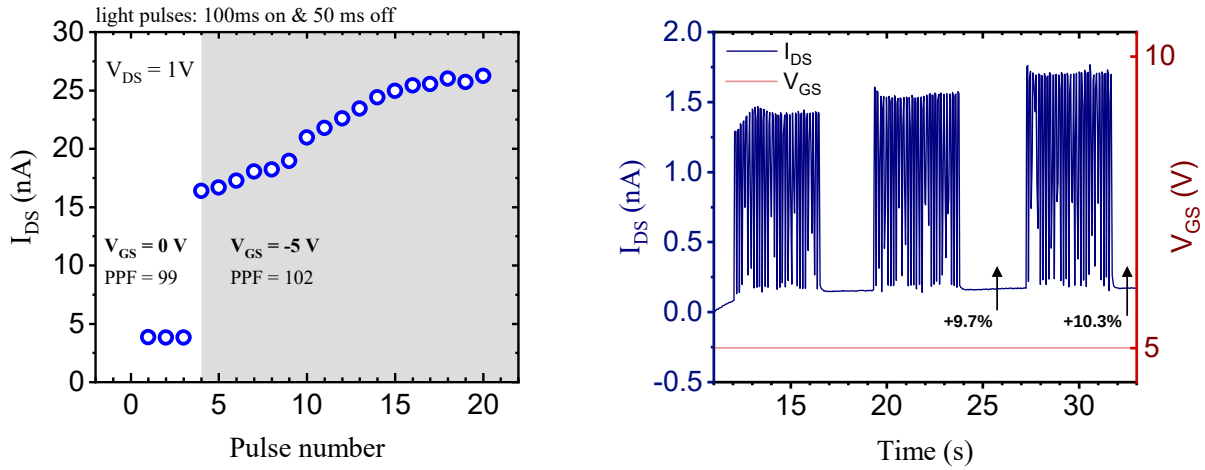

Figure 4.30: Measurement under 6.9mW/cm^2 light pulses (100ms on, 50ms off) of the 100 nm x 50 nm channel. a) *Post-synaptic current as a function of the light pulse number. The first three light pulses are applied without the application of gate voltage and no enhancement of the post-synaptic current is observed (PPF=99). After three light pulses a continuous gate voltage is also applied of V_G = -5V. The current increases after each pulse reaching 1.61 times higher at the last pulse.* ***b)*** *application of three groups of 30 light pulses with 3 sec time duration between each group. Each group starts with a higher value of post-synaptic current compared to the previous group. The base current after the second and third groups is 9.7% and 10.3% higher, respectively compared to the base current after the first group.*

The LTP mechanism can be demonstrated when a large number of input pulses are applied under light illumination. In **Figure 4.30b** it is seen that by applying three groups of 30 light pulses the post-synaptic current of each group is higher than its previous group, demonstrating the LTP mechanism, as the device "remembers" its previous conductance state and starts at a

higher level when the device is stimulated again. In particular, the current of the first pulse of the third group is 36.7% higher compared to the first one of the first group and 9.4% higher compared to the first pulse of the second group. Also, an increase of 9.7% and 10.3% is observed for the base current after the second and the third group, respectively, compared to the base current after the first group, demonstrating also the LTP mechanism.

The study of the dependence of the PPF factor by the time interval was also conducted, by applying three light pulses with 100 ms duration 1.72 mW/cm^2 intensity and different time intervals, 50 ms, 80 ms, 120 ms 150 ms and 200 ms, as shown in **Figure 4.31a-e**. **Figure 4.31f** summarizes the calculated PPF factor of each measurement and shows that it generally decreases as the time interval increases. In particular, the time intervals of 50 ms and 80 ms result in the same PPF factor of 103, while the 120 ms results in PPF factor of 101 and for the 150 ms it increases at the value of 102. The big difference arises for the time interval of 200 ms which results in a PPF factor of 95 showing that the modulation of the postsynaptic current is not achieved anymore. This is reasonable, as the iodide vacancies generated by the light pulse have enough time to diffuse back and recombine with the iodine anions when the time duration between the pulses is long.

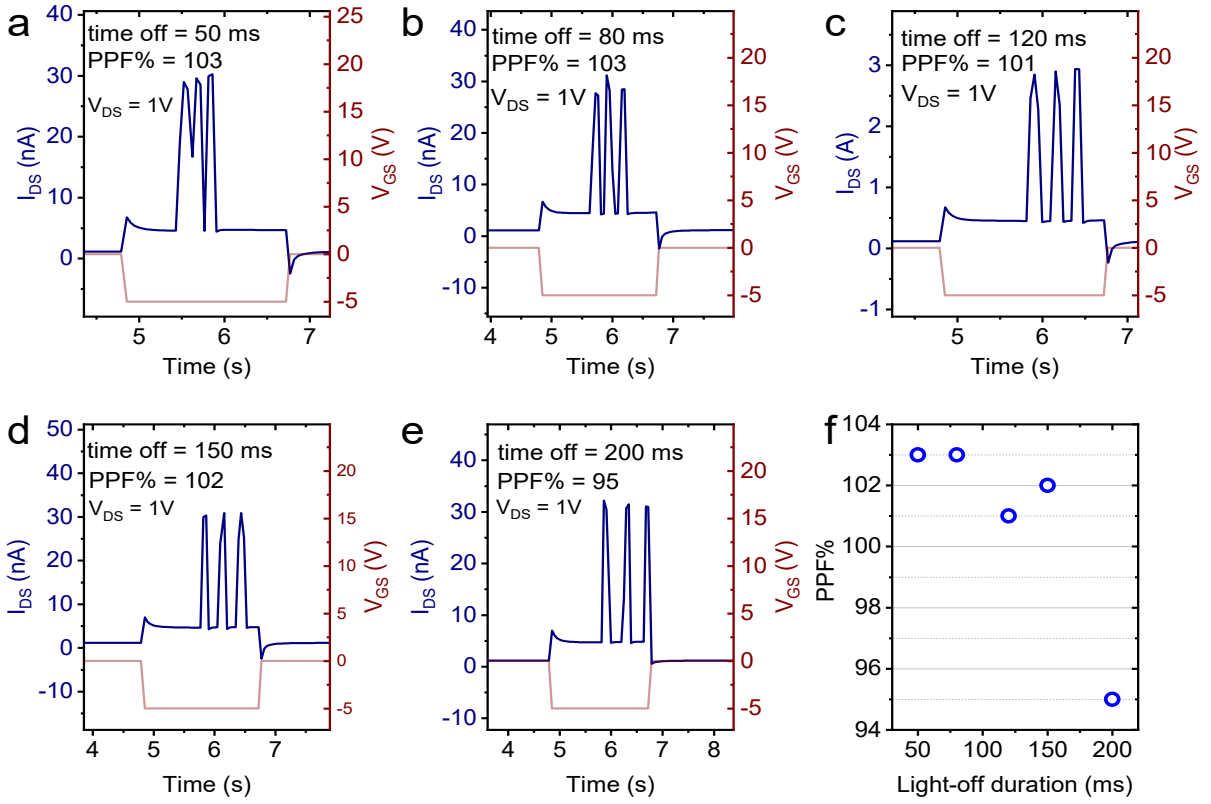

Figure 4.31: Study of the PPF factor as a function of time interval between light pulses. *Light intensity was 1.72 mW/cm^2. During the light pulses the gate voltage was V_G = -5V. Time interval was set to* ***a)*** *50ms, PPF=103 calculated,* ***b)*** *80ms, PPF=103 calculated,* ***c)*** *120ms, PPF=101 calculated,*

d) *150ms, PPF=102 calculated,* ***e)*** *200ms, PPF=95 calculated.* ***f)*** *PPF factor as a function of time interval between light pulses.*

4.6.5 Linearity of conductance states update

The high linearity of the conductance states update is also important and highly desirable for neuromorphic computing. Typically, high nonlinearity results in complex weight updates and increased energy and time consumption during the training process. Conversely, a linear and symmetric weight update behavior with a sufficient number of states can significantly enhance the inference accuracy and reliability of neuromorphic computing [118]. Thus, improving the linearity and symmetry of an artificial synapse device is crucial for developing a low-power, high-accuracy artificial neuromorphic network [119].

For the quantitative analysis of the linearity of the conductance state update, the nonlinearity factor (ν) is employed [119], [120], which indicates the nonlinear behavior of the conductance update. It can be calculated based on the normalized conductance, G_P, as a function of the normalized pulse number, p. The normalization of the above terms occurs by dividing them by their maximum value. A nonlinearity factor with a value close to zero corresponds to a less nonlinear relation.

The equation that describes the G_P in the function of the p, for the LTP process, is as follows:

$$G_P = G_{min} + B(1 - e^{-\nu p})$$

where G_{min} is the minimum normalized conductance, ν is the nonlinearity factor, p is the normalized pulse number and B is a constant [119].

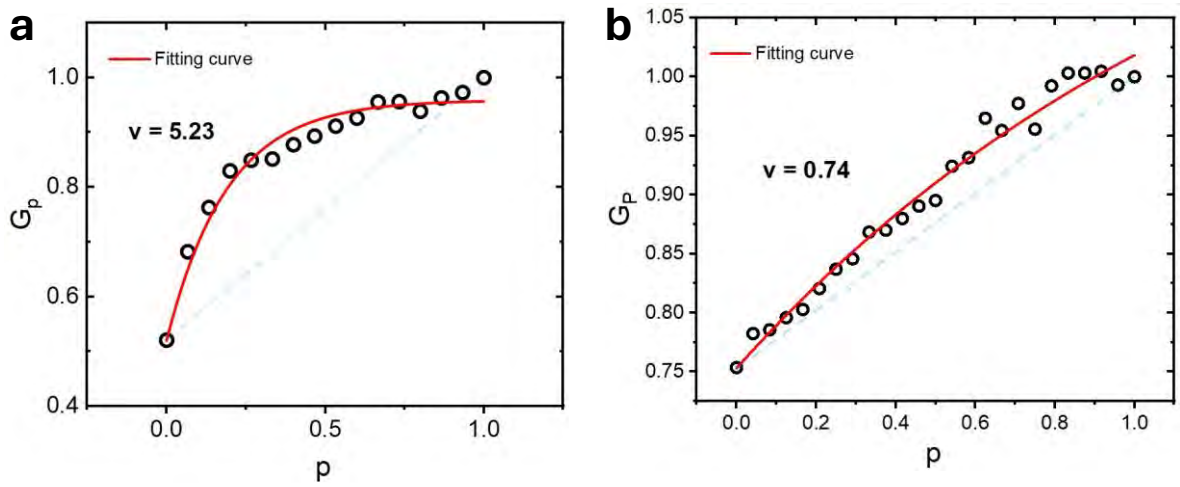

Figure 4.32: Effect of light illumination on the linearity of conductance states on the bottom-gate transistor with ALD-AlOx dielectric. a) *normalized conductance as a function of normalized pulse number without light illumination. The nonlinearity factor is extracted from the fitting curve as ν = 5.23.* ***b)*** *normalized conductance as a function of normalized pulse number. Measurements under light*

illumination. The nonlinearity factor is extracted from the fitting curve as ν = 0.74. The dotted line corresponds to the ideal linear behavior.

The **Figure 4.32a** displays the plot of normalized conductance states as a function of the normalized pulse number for the bottom-gate transistor with AlOx ALD dielectric, using the data from the **Figure 4.22**. The **Figure 4.32b** shows a measurement of the same device under light illumination. By fitting the data with the above equation, the nonlinear factor is extracted as: ν = 5.23 without illumination and ν = 0.74 under illumination. This demonstrates that light illumination significantly improves the linear conductance state update.

Similar behavior is observed for the substrate-as-gate transistor. The data used for the fitting are those of **Figure 4.18d** and **Figure 4.28** for non-illuminated and illuminated measurements, respectively. For the data of **Figure 4.18d.** the fitting equation has to be modified, as the behavior of the conductance update is exponential. The following equation is proposed for this reason, which shows to follow the experimental data, as depicted in **Figure 4.33a**:

$$G_P = G_{min} + B(e^{vp} - 1)$$

The extracted nonlinear factor is 3.11, for the non-illuminated device, and 1.58 for the illuminated one, showing again the improvement in linearity of the conductance states under light exposure.

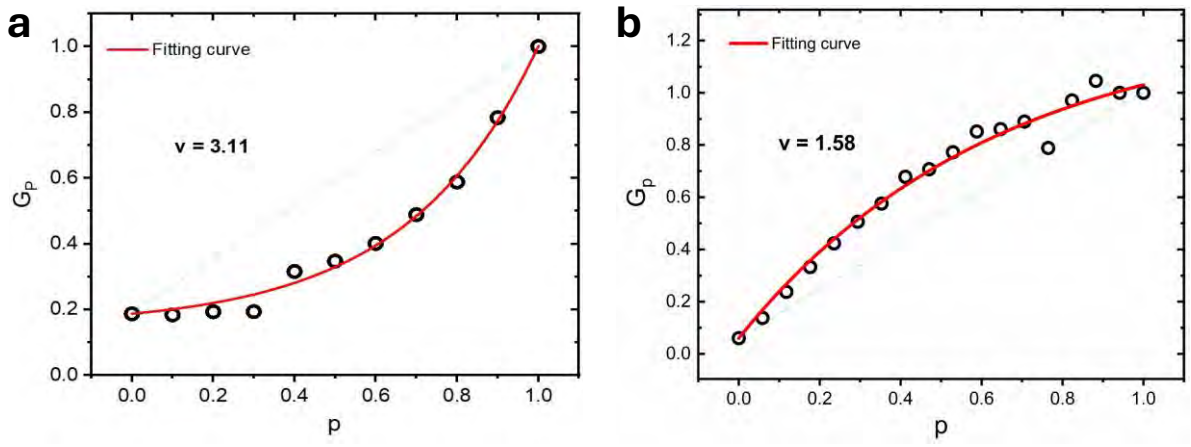

Figure 4.33: Effect of light illumination on the linearity of conductance states on the substrate-as-gate transistor. a) *normalized conductance as a function of normalized pulse number without light illumination. The nonlinearity factor is extracted from the fitting curve as ν = 3.11.* ***b)*** *normalized conductance as a function of normalized pulse number. Measurements under light illumination. The nonlinearity factor is extracted from the fitting curve as ν = 1.58. Dotted line corresponds to the ideal linear behavior.*

4.6.6 Energy consumption calculations

The energy consumption per synaptic event, for synaptic transistors, can be calculated by the sum of two terms: the energy dissipated by the gate voltage pulse and the energy dissipated by the continuous reading drain-source voltage during the gate pulse [31], [121]. The first term is:

$$E_{GS} = V_{GS} \times I_{GS} \times t$$

where V_{GS} is the amplitude of the gate pulse, the I_{GS} is the peak-current during the pulse and t is the pulse duration. The energy provided by drain-source bias is:

$$E_{DS} = V_{DS} \times I_{DS} \times t$$

where V_{DS} is the applied continuous drain-source bias, I_{DS} is the peak-current of the channel during the gate pulse and t is the duration of the gate pulse. Usually, the first term is negligible as the gate-source current is orders of magnitudes lower than the current of the channel. The devices in this work have a big leakage current, comparable to the drain-source current, thus the energy dissipated by the gate pulse is also considered in the calculations.

For the substrate-as-gate configuration, in the device with channel dimensions $10\mu m \times 1\mu m$, the energy consumption is calculated 5.53 nJ per synaptic event for a gate pulse of 5V, and 50ms duration and 7.86 nJ per synaptic event for a gate pulse of 5V and 100 ms duration.

For the bottom-gate transistor configuration, for a smaller channel dimension of $100nm \times 50nm$ lower energy consumption is calculated at 0.95 nJ per synaptic event for a 5V and 50 ms gate pulse and 4.36 nJ per synaptic event for 7V and 100 ms gate pulse.

For the bottom-gate transistor with AlOx – Sol-Gel dielectric, for a channel with dimension of $100nm \times 50nm$ it was calculated at 1.35 nJ per synaptic event for 2V and 100 ms gate pulse and 393 nJ per synaptic event for 10V and 100 ms gate pulse.

Under light illumination measurements, the energy dissipated by the light source has also to be included and can be calculated by the term:

$$E_{light} = I \times A \times t$$

where I is the light intensity, A is the surface area of the channel and t is the duration of the gate pulse, or the duration of the light pulse, in case of pulsed measurements. In general, the energy by the light source is very low, in the order of femto-joules. For example, for the measurements in the bottom-gate transistor with ALD-AlOx dielectric, where light intensity was 0.8 mW/cm^2, on channel dimensions $100nm \times 50nm$, (yielding a 5 x 10^{-11} cm^2 channel surface area), and with a 100 ms gate pulse duration, it results in E_{light} = 4 fJ per synaptic event,

which is extremely low. However, the energy consumption of the other two terms, the drain-source voltage and the gate pulse are higher resulting in an energy consumption of 8.5 nJ per synaptic event for a gate pulse of 5V and 100 ms duration. The above calculations correspond to the measurements in **Figure 4.26**.

For light-pulse the light intensity was 6.9 mW/cm^2 and 100 ms duration, the energy by the light is calculated: $E_{light} = 34.5$ fJ per synaptic event, while the total energy resulted in 2.47 nJ per synaptic event for the measurements of **Figure 4.30**.

The energy consumption of the devices diverges from the biological level of 1-100 fJ per synaptic event. This is attributed mostly to the high leakage current of the device, resulting in the high value of the term E_G. These results are promising for light-stimulated artificial synapses. Lowering the leakage current and picking a lower source-drain voltage to get a lower source-drain current could help to bring the total energy consumption down to values close to that of biological synapses

4.6.7 Comparison with the literature

In general, both device configurations, fabricated in this work, demonstrated synaptic characteristics either by solely electrical stimulation or by the combination of both electrical and light stimulation. The PPF factor, the gain (ratio of the synaptic currents A_{10}/A_1), and the nonlinearity factor can be used for quantitative analysis and comparison of the different devices' performance. The calculation of energy consumption is also very important for the utilization of devices in low-power-consuming neuromorphic hardware. It is noteworthy to compare the performance of this work's devices with the existing works in literature. In this section, firstly the comparison of the synaptic transistors that work solely with electrical stimulation is discussed and then the comparison of the photo-synaptic transistors follows.

4.6.7.1 Synaptic transistors

Only three studies [30], [36], [37] in the literature have explored perovskite synaptic transistors that operate solely with electrical stimulation. In two of them [36], [37], pre-synaptic pulses are applied using the drain and source electrodes (V_{DS}), and a continuous gate voltage (V_{GS}) is used to modulate conductance states. This measurement protocol contrasts with the typical approach in synaptic transistors, where gate pulses serve as the pre-synaptic stimulus and a low continuous drain-source voltage is applied to read the channel current. The latter method, which

is also used in this work, as well as in the work of Jeong et al. [30] is considered more energy-efficient [30].

Table I summarizes the performance characteristics of various studies, with perovskite synaptic transistors that operate solely with electrical stimulation, including, also, two works on organic synaptic transistors for comparison [42], [40]. As shown, all devices in the literature have channel dimensions in the millimeter or micrometer range, whereas the devices in this work achieve dimensions in the nanometer range (e.g. 100 nm x 50 nm). Although one organic synaptic transistor has a channel length of 300 nm [42], it is still longer than those in this study. These findings indicate that the techniques presented in this thesis can effectively downscale device dimensions, resulting in functional synaptic devices. This level of miniaturization is highly desirable as it further reduces energy consumption and allows dense integration of the devices on chips.

The gain (A_{10}/A_1) of the devices in this study is generally lower compared to the literature, where values can reach up to 100 [30]. The highest gain achieved in this work is 10.9, measured on the substrate-as-gate transistor. Similarly, the paired-pulse facilitation (PPF) factor is relatively low compared to the highest literature's reported value of ~150 [36], for perovskite synaptic transistors. However, by pre-poling the substrate-as-gate device, a PPF factor of 197 can be achieved, as presented in **Figure 4.19**, surpassing all reported values in the literature.

The energy consumption of the devices in this study is significantly lower than that of existing perovskite synaptic transistors in the literature [30], [36], [37], as shown in **Table I**. The authors of those studies do not report energy consumption, however, estimated values for those devices are in the microjoule (μJ) range, if for the calculation of the energy consumption only the E_{DS} component of the drain-source voltage, is considered. In contrast, this work reports energy consumption of 5.53 nJ, 0.95 nJ, and 1.35 nJ for the substrate-as-gate transistor, bottom-gate transistor with AlOx ALD, and bottom-gate transistor with AlOx Sol-Gel, respectively, as calculated in section **4.6.6** , considering both E_{GS} and E_{DS} contributions. Despite similar voltage amplitudes and pulse durations across studies, the lower energy consumption in this work can be attributed to smaller channel dimensions and the specific perovskite material used. Further reductions in voltage amplitude and pulse duration could decrease energy consumption to the femtojoule (fJ) level. For instance, energy consumption between 1-100 fJ could be achieved with a pulse amplitude of 50 mV and a pulse duration of 0.5 ms.

Table I: *Comparison of Synaptic Transistors*

Channel Material	Device type	Channel dimensions (length x width)	Voltage, pulse duration	Gain (A_{10}/A_1)	PPF (A_1/A_2)x100	Energy per synaptic event	Ref.
$MAPb(I_{1-x}Br_x)_3$	transistor	30μm x 1cm	-20, 500ms	5.5	<100	~μJ (E_{DS})	[37]
$(MA_{0.15}FA_{0.85})Pb(I_{0.9}Br_{0.10})_3$	transistor	30mm x 50μm	5V, 100ms	28	<150	~μJ (E_{DS})	[36]
$CsPbBr_3$	transistor	25μm x 5mm	-30V, 20ms	>75	135	~nJ (E_{DS})	[30]
organic core-sheath nanowire	transistor	300nm	20mV, 111.2ms	3.33	~162	0.29 fJ (E_{DS})	[42]
stacked hybrid organic/inorganic ECRAM	transistor	15μm x 45μm	1μs	<2		2.71 pJ (E_{DS})	[78]
$MAPbI_3$ (This Work)	substrate-as-gate transistor	1mm x 10μm	5V, 50ms	10.9	197	5.53 nJ (E_{DS}+E_{GS})	**This work**
$MAPbI_3$ (This Work)	bottom-gate transistor (AlOx-ALD)	100nm x 50nm	5V, 50ms	1.4	112	0.95 nJ (E_{DS}+E_{GS})	**This work**
$MAPbI_3$ (This Work)	bottom-gate transistor (AlOx-Sol-gel)	100nm x 50nm	5V, 50ms	1.15	104	1.35 nJ (E_{DS}+E_{GS})	**This work**

For organic synaptic transistors, energy values of 0.29 fJ [42] and 2.71 pJ [78] have been achieved, approaching biological levels. However, for the calculations of the energy consumption, only the energy consumption, E_{DS}, of the continuous reading voltage (V_{DS}) has been taken into account excluding the energy consumption E_{GS} of the gate-source voltage (V_{GS}), being a limitation in their energy consumption calculation and therefore the above numbers do not reflect the actual energy consumption. The devices in this study could also reach these levels of energy consumption if leakage current is also reduced. Typical leakage currents in transistor devices are in the picoampere (pA) range, whereas in this study, they are in the nanoampere (nA) range. If the E_{GS} contribution to the total energy consumption is excluded, an energy consumption in the pJ range could be achieved. In particular, 25 pJ per

synaptic event for the bottom-gate transistor with AlOx-ALD dielectric, 153 pJ for the bottom-gate transistor with AlOx-sol-gel dielectric, and 530 pJ per synaptic event for the substrate-as-gate transistor, approaching the energy consumption of the organic-synaptic transistors.

4.6.7.2 Photo-synaptic transistors

Organic-halide perovskites have generally been used in photo-synaptic transistors as floating gate materials, as discussed in detail in the section **2.2.3** . This architecture involves a more complex fabrication process and typically results in higher energy consumption. Only two studies [33], [34], have used perovskite material directly in the transistor channel for photo-synaptic transistors. The first study employed a blend of $CsPbBr_3$ quantum dots and DPPDTT materials as the channel material, achieving the lowest energy consumption of 0.5 fJ, as reported by Hao et al. [33], with a channel size of 30 μm x 1 mm, when they applied a very low drain-source reading voltage (V_{DS}) of -0.0005V [33]. However, the authors only include the contribution of V_{DS} in the energy consumption, neglecting the energy consumption of the light pulse, which is calculated as $E_{light} = I \times A \times t$, resulting in 0.95nJ energy consumption for light intensity I = 0.05 mW/cm^2, channel area A = 3x10^{-4} cm^2 and pulse duration t = 50 ms. In the second study, the two-dimensional (2D) $(PEA)_2SnI_4$ perovskite was incorporated into the channel, with an estimated energy consumption of 44.8 nJ per synaptic event [34], as depicted in **Table II**.

In comparison, the devices in this work demonstrated an energy consumption of 5.53 nJ when stimulated by light pulses combined with a continuous gate voltage bias, and 8.5 nJ per synaptic event for continuous light illumination combined with gate pulses in bottom-gate transistors. For the substrate-as-gate transistor, an energy consumption of 45.7 nJ was calculated for continuous light illumination and gate pulses stimulation. These higher values are attributed to the higher intensity of light and longer pulse duration used in this study compared to those in the literature, as shown in **Table II**. However, it is noted that the contribution of the gate voltage in the energy consumption, in this work, is high, in the order of nA, while the energy consumption of the light source is calculated to the fJ level, due to the very small channel area. This suggests that achieving pA-level leakage current, by improving the dielectric layer, could reduce energy consumption to the fJ biological energy level. Studies on photo-synaptic transistors with perovskites as floating gates report relatively high energy consumption, ranging from 25 μJ (E_{DS} + E_{light}) [41], 80 nJ (E_{DS} + E_{light}) [84] to 13.5 pJ (E_{DS} + E_{light}) [122], as shown in **Table II**.

***Table II**: Comparison of Optoelectronic Synaptic Transistors*

Channel Material	Device type	Channel dimensions (length x width)	Light intensity, pulse duration	Gain (A_{10}/A_1)	PPF (A_1/A_2)x100	Energy per synaptic event	Ref.
$CsPbBr_3$ QDs/ pentacene	Floating gate transistor	1mm x 50μm	0.153 mW/cm^2, 1s V_{DS} = 0.2V	1.39	130	80 nJ (E_{DS}+E_{light})	[84]
Si NM on $MAPbI_3$	floating gate transistor	25μm x 500μm	1μW/cm^2, 200ms V_{DS} = 0.01V	1.44	168	13.5 pJ (E_{DS}+E_{light})	[122]
Blend of DPPDTT and $CsPbBr_3$ QD	transistor	30μm x 1mm	450 nm, 0.05mW/cm^2, 50ms V_{DS} = -0.0005 V	1.22	105	0.95 nJ (E_{DS}+E_{light})	[33]
$Cs_3Bi_2I_9$ NCs/ DPPDTT	floating gate transistor	2.5cm x 20μm	0.1mW/cm^2, 50ms		104	25 μJ (E_{light})	[41]
2D $(PEA)_2SnI_4$	transistor	7μm x 50 μm	11.6 μW /cm^2, 20ms V_{DS} = 2V	1.69	130	44.8 nJ (E_{DS}+ E_{light})	[34]
$MAPbI_3$ (This Work)	bottom-gate transistor (AlOx-ALD)	100nm x 50nm	6.9mW/cm^2, 100ms V_{GS} = -5V, 50ms V_{DS} = -1V (light-pulse)	1.47	102	5.53 nJ (E_{DS}+E_{GS}+ E_{light})	**This work**
$MAPbI_3$ (This Work)	bottom-gate transistor (AlOx-ALD)	100nm x 50nm	0.8mW/cm^2 V_{GS} = -5V, 50ms V_{DS} = -1V (continuous light)	1.12	100	8.5 nJ (E_{DS}+E_{GS}+ E_{light})	**This work**
$MAPbI_3$ (This Work)	substrate-as-gate transistor	10μm x 500nm	80mW/cm^2 V_{GS} = -5V, 50ms V_{DS} = -1V (continuous light)	6.19	173	45.7nJ (E_{DS}+E_{GS}+ E_{light})	**This work**

Furthermore, all devices have channel dimensions from cm to μm order of magnitude, as shown in **Table II**, compared to the devices of this work that reach down to the nm range (i.e. length x width = 100nm x 50nm). The above indicates that the fabrication techniques presented in this thesis can be used for downscaling the devices' dimensions and achieve a functional device, being a significant contribution to the scientific literature for this research topic.

The PPF factor for the bottom-gate transistor in this work is lower than those reported in the literature, but for the substrate-as-gate transistor, it is significantly higher at 173, compared to

all reported values ranging from 104 to 168, as depicted in **Table II**. The gain (A_{10}/A_1) of the bottom-gate transistor in this work is comparable to those in the literature, while for the substrate-as-gate transistor, the gain is 4 to 5 times higher at 6.19, compared to all literature values where it ranges from 1.22 [33] to 1.69 [34], as shown in **Table II**.

These results demonstrate that downscale devices can exhibit synaptic functions with relatively similar performance to those in the literature. Additionally, these devices can exhibit photo-synaptic characteristics without needing a floating gate, simplifying the device architecture. This represents an important contribution to the field, addressing the need for simpler devices with direct perovskite use in the transistor channel, as reported in [35].

Chapter 5

Conclusions & Outlook

Conclusions

This thesis investigated the potential of hybrid organic-inorganic metal halide perovskites for low-energy synaptic applications within neuromorphic hardware. The study explored the fabrication and electrical characterization of downscale synaptic-transistor devices using $MAPbI_3$ perovskite as the channel material, aiming to achieve ultra-low power consumption. The findings revealed that both the substrate-as-gate and bottom-gate transistor architectures exhibited promising synaptic characteristics by both light and electrical stimulation.

The research gaps, in the scientific literature, presented in the section **1.3** , have been addressed through this work and the results provide insightful knowledge. First, a significant gap in the current research is the lack of studies focusing on the miniaturization of channel dimensions in synaptic transistors, which leads to lower energy consumption and allows their integration on chips, in high density. In this work, the miniaturization of the devices' dimensions on the nano-level scale has been successfully demonstrated, with two different proposed device architectures (substrate-as-gate transistor and bottom-gate transistor). Electrical characterization of those devices revealed that they can demonstrate synaptic functions, such as STP, LTP, and LTD, by both electrical and light stimulation.

The dual-mode stimulation (electric and light) of those devices is a significant advantage over many other artificial synapses, that are solely electrically stimulated. The light stimulus offers a significant reduction in energy consumption and adds one further dimension to the operation of these devices, showing the potential for utilization of those devices in more efficient and flexible neuromorphic computing systems, for example, in-sensor computing.

This work also fulfills the demand for simplified architectures of photonic-synaptic transistors, as current works in the literature use the perovskite as a floating-gate component in the device

which leads to more complex architecture and higher energy consumption. In this work, the halide perovskite material ($MAPbI_3$) is directly deposited on the transistor channels, and the devices successfully show synaptic functions. This significantly adds to this area of research by providing a more straightforward and energy-efficient alternative.

Finally, there is a notable lack of studies on the energy consumption of perovskite synaptic transistors that work solely by electrical stimulation. In this work, the devices demonstrated synaptic characteristics through electrical stimulation and the energy consumption has been addressed. This contribution is crucial for understanding and optimizing the performance of perovskite synaptic transistors in neuromorphic applications.

The comparative analysis of the experimental results with the existing works in the literature showed the advantages and the limitations of the devices in this work, which gives space for further optimizations in future studies. For the electrically stimulated devices, the gain (A_{10}/A_1) has been compared to the literature, where values can reach up to 100. The highest gain achieved in this work is 10.9, observed in the substrate-as-gate transistor. Additionally, the paired-pulse facilitation (PPF) factor is relatively low compared to the highest reported value of ~150 for perovskite synaptic transistors. However, by pre-poling the substrate-as-gate device, a PPF factor of 197 can be achieved, surpassing all reported values in the literature. The devices in this study have significantly lower energy consumption compared to existing perovskite synaptic transistors, which have estimated values in the microjoule (μJ) range. This work reports energy consumption of 5.53 nJ, 0.95 nJ, and 1.35 nJ for different transistor configurations. The lower energy use is due to smaller channel dimensions and specific perovskite materials. In theory, further reductions in the voltage amplitude of the gate pulse, the pulse duration, the drain-source reading voltage, and the leakage current, could lower energy consumption to the femtojoule (fJ) level, potentially achieving 1-100 fJ. For example a gate dielectric with lower leakage current and higher dielectric constant would have higher capacitance, achieving stronger accumulations of charge carriers in the channel, significantly reducing the gate voltage. If the E_{GS} contribution in the total energy consumption is excluded, as most authors do in their works, energy consumption in the pJ range can be achieved, 25 pJ per synaptic event for the bottom-gate transistor with AlOx-ALD dielectric, 153 pJ for the bottom-gate transistor with AlOx-sol-gel dielectric and 530 pJ per synaptic event for the substrate-as-gate transistor, approaching the energy consumption of the organic-synaptic transistors.

For the photo-synaptic transistors, only two studies have used perovskite directly in the transistor channel, achieving energy consumption of 0.95 nJ and 44.8 nJ per synaptic event. In comparison, this work demonstrates energy consumption of 5.53 nJ with light pulses and continuous gate voltage stimulation, and 8.5 nJ per synaptic event with continuous light and gate pulses stimulation in bottom-gate transistors. The substrate-as-gate transistor shows 45.7 nJ under similar conditions. These higher values are due to higher light intensity and longer pulse duration. Reducing the light intensity, and the gate voltage amplitude and improving the dielectric layer could lower energy consumption to the femtojoule level. Studies with floating-gate configurations, which are more complex architectures, reasonably report higher energy consumption, ranging from 25 μJ to 23.5 pJ.

The PPF factor for the bottom-gate transistor in this work is lower than those in the literature, but the substrate-as-gate transistor shows a significantly higher PPF factor of 173, compared to reported values that range from 104 to 168. The gain (A_{10}/A_1) of the bottom-gate transistor in this work is comparable to literature values, while the substrate-as-gate transistor, in this work, has a gain of 6.19, which is approximately 5 times higher than the reported range of 1.22 to 1.69.

Finally, it is noteworthy that the devices demonstrated increased linearity in the conductance state updates under light illumination, with the lowest nonlinear factor obtained for the substrate-as-gate transistor with the value $\nu = 0.29$. Linearity is highly desirable when those devices are used in neuromorphic applications as it enhances significantly the accuracy and reliability of the calculations in those systems.

Outlook

Despite these promising results of the devices in this study, improvements in energy efficiency are required for these devices to compete with the low energy consumption of biological synapses and the previously demonstrated synaptic transistors based on other materials [42], [122]. One significant challenge is the high leakage current, particularly when the device is scaled down to nano-level. In the substrate-as-gate transistor, the thermal grown SiO_2 dielectric is not resistive enough, therefore this should be improved by adding HCl or Cl_2 during the thermal growth of the SiO_2. The poor resistivity of the bottom-gate transistor with the AlO_x dielectric layer deposited by the ALD method could be due to the large amount of unreacted

precursor during the deposition, so more experimental tests should be done to improve the quality and reduce the defects of the deposited layer. Also, as the AlOx dielectric deposited with the Sol-Gel method gives promising results in the device performance, further experimental studies should be done for the wetting improvement of the substrate, by the dielectric film. Future research could also focus on employing dielectrics with higher dielectric constants and lower leakage currents, such as HfO_x [123]. Such dielectrics can increase capacitance and lower the working bias of the device, thereby reducing energy consumption.

Additionally, systematic studies on the synaptic performance of these devices are necessary. Measurements with lower amplitude gate voltage pulses, lower intensity of the light source and shorter stimulation durations (pulse length) should be investigated, as this would further reduce energy consumption.

The positive effects of light illumination on synaptic performance, such as the enhancement of the paired-pulse facilitation (PPF) factor and improved linearity of conductance states, indicate a need for deeper exploration of optoelectronic interactions within these devices. Future studies could employ monochromatic light at various wavelengths to achieve better control of excitation characteristics and further improve the performance of perovskite-based synaptic transistors.

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Appendix

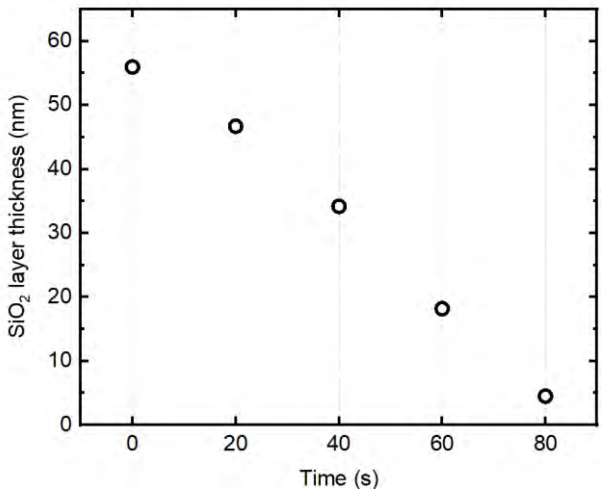

Figure A6. 1: *SiO_2 layer thickness versus etching time*

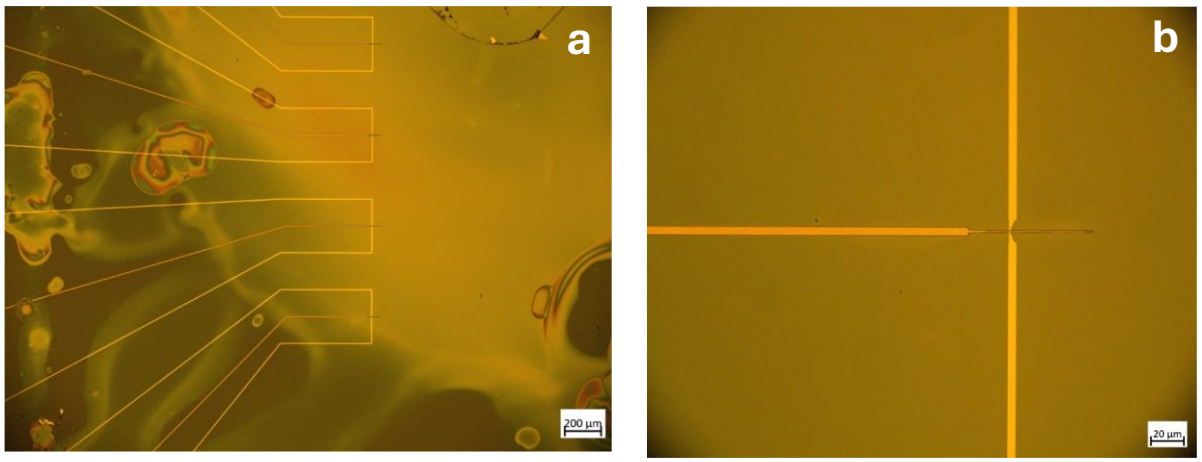

Figure A6. 2: *Optical microscope images.* ***a)*** *poor uniformity due to poor wetting during the deposition of the substrate by the Sol-Gel AlOx dielectric layer.* ***b)*** *higher magnification image of the channel region, where the dielectric film looks homogeneous.*

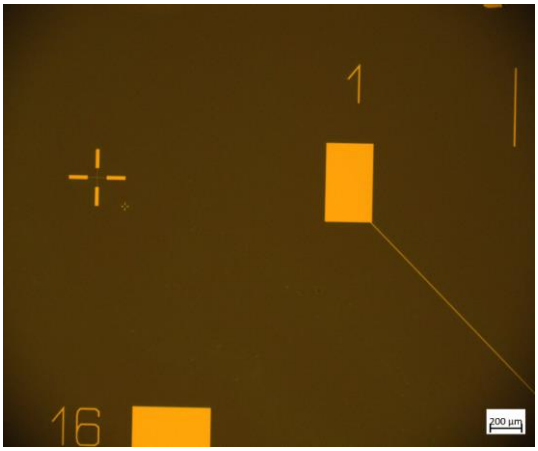

Figure A6. 3: *Optical microscope image of the bottom-gate transistor sample after the first lithography step and the patterning of gate electrodes. On the top-left, the crosses can be seen, used as a reference for the alignment of the drain and source electrodes over the gate electrode, during the second lithography step of the drain and source patterning. Gold rectangular features correspond to the contact pads of the gate electrodes.*

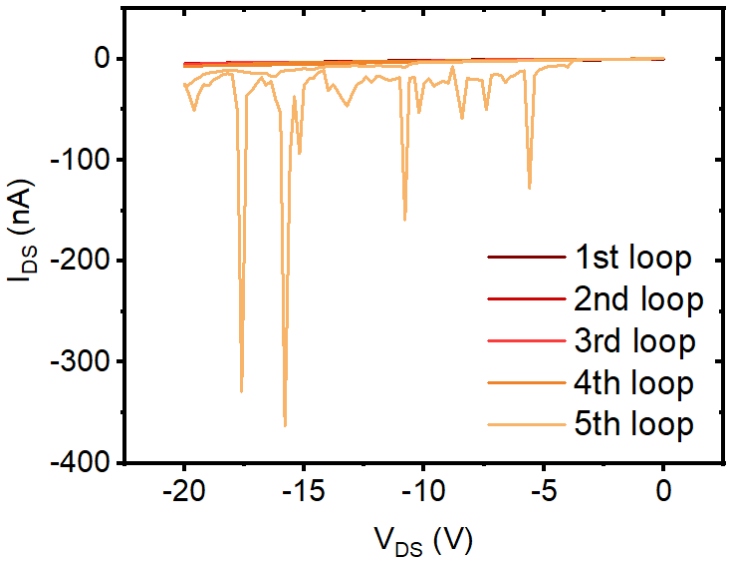

Figure A6. 4*: Full-scale plot of the single channel measurement corresponding to the measurements of* ***Figure 4.15b****, when consecutive negative voltage sweeps were applied.*