# Light Management in Perovskite Light-Emitting Diodes via Outcoupling Enhancement

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# Abstract

Light-Emitting Diodes (LEDs) are devices that emit light under an applied bias voltage and are essential to our current way of life as they provide most of the worlds artificially generated light. However, with the impending climate disaster looming over the horizon, global energy consumption needs to be reduced as much as possible, including in the field of Solid-State Lighting. Therefore, the need for developing ever more efficient LEDs is high. A new class of materials called Metal Halide Perovskites (MHPs) has emerged in the last decades as a popular candidate for the next generation of LEDs. However, the system still experiences severe losses due to Total Internal Reflection (TIR), which severely limits the achievable efficiency. In this work, a nanopatterned interstitial layer is inserted in a typical perovskite LED (PeLED) device stack using soft conformal imprint lithography (SCIL) that has been shown to reduce the fraction of light lost due to TIR by scattering the waveguided photons. However, due to issues regarding the patterning procedure and quality of the Hole Transport Layer (HTL), more work is needed to conclude the effectiveness of the method to enhance the outcoupling efficiency of the device.

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# Glossary

LED – Light-Emitting Diode

PeLED – Perovskite Light-Emitting Diode

EL – Electroluminescence

PL – Photoluminescence

EQE – External Quantum Efficiency

IQE – Internal Quantum Efficiency

OCE – Outcoupling Efficiency

TIR – Total Internal Reflection

ETL – Electron Transport Layer

HTL – Hole Transport Layer

ITO – Indium Tin Oxide

PVK – Polyvinylcarbazole

MHP – Metal Halide Perovskite

SCIL – Soft Conformal Imprint Lithography

AFM – Atomic Force Microscopy

SEM – Scanning Electron Microscopy

JVL – Current Voltage Luminance

# 1. An Introduction to Perovskite LEDs

The impending climate disaster is quite possibly the biggest challenge that humanity will have to face in the coming decades, as already extreme weather patterns are observed all around the world which endanger the lives of millions of people. One of the root causes to this problem is the ever-increasing need for more energy to be consumed around the globe, a large fraction (≈20%) of which is used in the form of electricity for a variety of purposes [15]. Around 15-20% of this energy is expended for the use of artificial lighting purposes, for both the residential and commercial sector [14]. More efficient use of this significant fraction of the electricity allows us to make a small but meaningful contribution to the necessary revolution of energy consumption in the future.

Light Emitting Diode (LED) technology has already revolutionized the field of Solid-State Lighting (SSL) in the last decades. Since the start of its industrial production around the 1960s it has overtaken the market and now accounts for more than 50% of the total consumption of electricity for SSL, which is expected to grow even more in the next coming years [16]. It is used in various essential commercial applications beyond general lighting purposes such as displays and medical devices, and the need for developing ever increasing efficiency and utility is high.

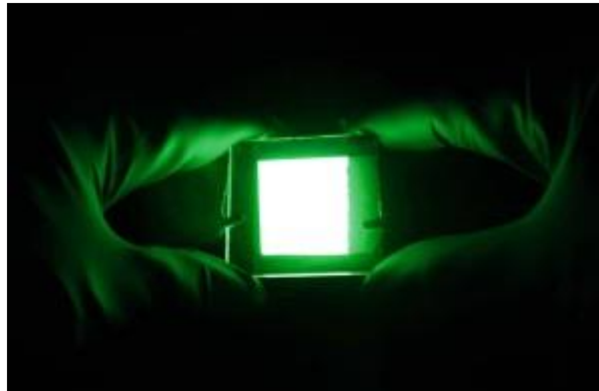

*Figure 1.1: A picture of a green perovskite LED in operation [3].*

One such development in the last decade is the introduction of a new class of materials as the light emitting component, called Metal Halide Perovskites (MHPs), often just denoted as perovskites. These materials possess a variety of advantageous optoelectronic properties when compared to conventional LED technology, such as low-cost scalable fabrication methods, high colour purity, facile composition & morphology tunability and a highly adjustable bandgap, that makes them a popular candidate for the next generation of LEDs [17].

However, as the field of perovskite LEDs (PeLEDs) has not yet fully matured, there are still some challenges that need to be overcome for it to reach its full potential. One such obstacle is the massive efficiency losses accrued by the Total Internal Reflection (TIR) of generated light due to the large difference in reflective index between the various materials within the device [9]. It is known that the insertion of a (periodic) nanopattern between the respective device layers can be used to scatter the light trapped by TIR and thus increase the fraction of photons escaping from the LED, thereby enhancing the overall efficiency [18-24,28].

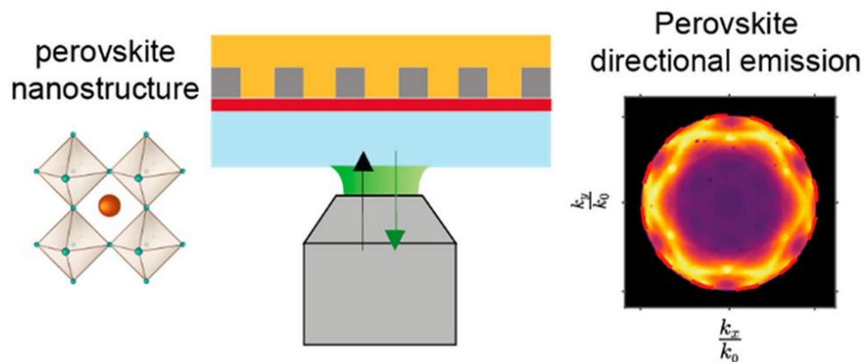


*Figure 1.2: An excerpt of the publication by Muscarella & Cordaro et al. showing the perovskite nanostructure (left), a schematic representation of the layered PeLED under investigation (middle) and some of the Fourier microscopy results that exhibit a preferred directional light emission (right). [2]*

A lot of unknows are still present in this active area of research and manufacturing a fully functioning LED to accurately study this effect is far from trivial, as the device consists of various layers that need to be of a high quality and integrated well to properly function. An example of this is seen in a previous publication [2] which inspired this work, where the authors were able to show a remarkable directional increase in photoluminescent emission of a PeLED device by indirectly patterning the perovskite layer with an interstitial silica-based nano-hole array using a specially developed imprinting method. However, they were unable to include the electroluminescent properties due to poor device efficiency. A summary of this work is shown in **Figure 1.2**.

Therefore, the aim of this project is to manufacture a functioning PeLED device using the methods and knowledge gained from this article and reproduce the results with electroluminescent emission instead. This is done in collaboration with Cambridge University, as they have shown remarkably efficient PeLED devices using a similar architecture.

The theoretical background necessary for understanding this report will be provided in chapter 2. Chapter 3 will outline the experimental methods used to fabricate and characterize the PeLED devices, the results of which will then be presented and discussed in chapter 4. Finally, chapter 5 will provide a summary and conclusions of the most important findings presented in this report.

# 2. Theoretical Background

This chapter will provide the theoretical framework necessary to understand the goals of the project and the steps made to get there. First-off a short introduction on the topic of LEDs, their typical device structure, and figures of merit. Afterwards the focus will be on the perovskite class of materials, in particular the specific type used in this work, its unique properties and how they can be functionalized for effective integration into PeLEDs. Finally, a discussion on the light management of PeLEDs will follow by highlighting one of the main current problems and possible solution explored in this work.

## 2.1 Light-Emitting Diodes

As mentioned in **Ch.1**, energy consumption is an important topic for the future of our society, and lighting is (and will probably remain) a significant part of global electricity usage [15]. Therefore, it is important to use this energy as efficiently as possible and further improve the overall efficiency of LEDs, which account for the majority of energy consumption for lighting purposes. This chapter will introduce their general working principles and important parameters that can be used to evaluate and compare their performance.

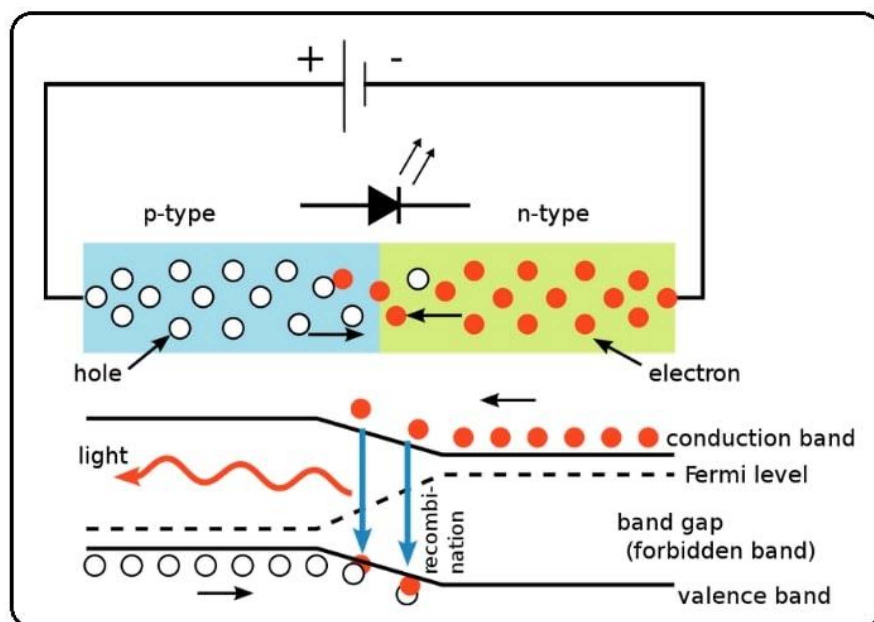


*Figure 2.1: A diagram showcasing the working principle of p/n junction LEDs, including the electrons and holes traveling through the circuit (top) and the representative band diagram (bottom) [4].*

Conventional light-emitting diodes, as their name implies, are diodes (essentially an electronic device which conducts current primarily in one direction) with the main function of emitting light (photons). To achieve this, a semiconductor material is usually utilized as an emissive material due to their (inherent) direct bandgap (the energy difference between the conduction and valance bands), which leads to the emission of narrow band light (called electroluminescence) anywhere in the range of Infrared (IR) to Ultraviolet (UV) under an applied bias voltage depending on the bandgap energy. This process occurs due to the radiative recombination of free carriers (electrons and holes) induced by the bias voltage [16].

To this end, an LED typically consists of a so-called p/n junction, as shown in **Figure 2.1**, where a p-doped (positively charged) & a n-doped (negatively charged) semiconductor are connected. This facilitates the movement of charge carriers across the interface, which can then recombine radiatively to emit photons around the bandgap energy.

A variation of this system is a p/i/n junction, which has an additional layer between the p and n regions called an intrinsic region that roughly contains an equal amount of positively and negatively charged carriers [26]. In this system charge carriers are injected into the intrinsic layer at the p and n interfaces, where they can recombine. This allows for an LED to function with an undoped semiconductor material, which still determines the emissive properties of the device and will be the device structure used in this work.

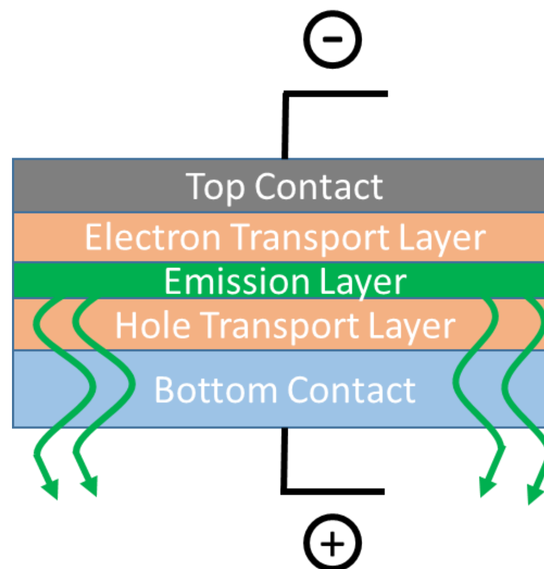


*Figure 2.2: A schematic representation of the different layers present in a typical p/i/n junction LED.*

A typical p/i/n junction LED architecture is shown in **Figure 2.2**. It consists of 5 main layers: 2 contacts, 2 Charge Transport Layers (CTLs) and an emission layer (which was previously discussed). The contacts are typically metals or metal oxides with a high conductivity, which allow for the electrons and holes to flow from the attached circuit into the device efficiently. CTLs, consisting of Electron and Hole Transport Layers (ETLs & HTLs) are usually inserted between the contacts and the emission layer for a wide variety of reasons. A few regularly reoccurring motivations are improving band alignment, maintaining charge balance, blocking opposite charges and preventing problematic reactions between the emission and contact layers, which help in improving the overall efficiency and lifetime of the device [27]. In this type of device stack, one of the contact and CTL pairs (Bottom & HTL in this figure) needs to be transparent for the emitted light to effectively travel out of the LED.

There are 3 main parameters in evaluating an LED's overall performance during normal operation: The Voltage (V), Current (I) and the emitted photons. This is an oversimplification as there are actually a lot more factors at play such as injected charge carrier balance, (non)-radiative recombination rates, PLQE, etc. [26]. However those will not be further investigated in this work so they are not relevant enough for a full discussion here.

The voltage (in Volt (V)) defines the force that is applied to the charge carriers that drives them to transfer to the intrinsic layer and thus allow for current to flow. The point where current starts to flow and light emission is observed is called the turn-on Voltage and is an important characteristic for LEDs, as it (in combination with the current) describes the energy barrier that charge carriers experience before recombining. The current (in Ampere (A)) is defined by the number of charge carriers flowing through the device and therefore is important in evaluating the overall efficiency of the LED as, in an ideal case, the number of photons emitted is equal to the number of charge carriers injected. This term is often represented as current density, which is simply the total amount of current divided by the area of the emissive layer, as to normalize the unit to be independent of LED size.

The last parameter is less straightforward and requires a bit more explanation, as there are a variety of ways to represent the photons emitted from an LED. Here the focus will be on a method to obtain the Efficiency and Luminance [1].

The unit that is initially obtained from so-called JVL measurements is the radiant intensity (R), which is the total power of the emitted photons per solid angle [W/sr]. This can be derived from the total induced current of the emitted light in a photodetector, which is a measure of the emissivity of the LED, by correcting for the responsivity of the detector and the geometry to determine the effective solid angle.

This radiance intensity can then be converted to a total photon flux ($\phi$), which is just the total number of photons per unit area per second, by dividing by the weighted photon energy average (which can be obtained from the normalized Electroluminescence spectrum) and expanding area to the entire forward hemisphere (which is just a multiplication by pi if Lambertian emission can be assumed).

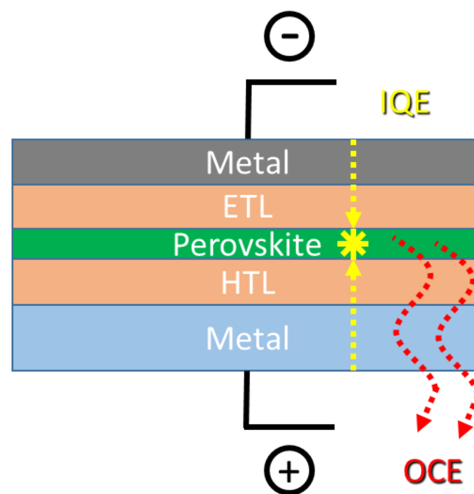


*Figure 2.3: A schematic representation of a PeLED that highlights 2 distinct processes that determine the EQE. The IQE (yellow) contains the injection and recombination of charge carriers and the OCE (red) contains the outcoupling of generated light into the far-field.*

Once $\phi$ is known, the External Quantum Efficiency can easily be obtained as it is defined as the ratio of outcoupled photons to the number of electrons flowing through the circuit (which is just the current divided by the elementary electron charge). This efficiency term can be split in 2 terms to describe 2 distinct processes happening within the LED (as shown in **Figure 2.3**), namely the Internal

Quantum Efficiency (IQE) and the Outcoupling Efficiency (OCE). Here the IQE describes the efficiency of injecting the charge carriers into the LED and combining radiatively to emit a photon (as seen in yellow) and the OCE describes the efficiency of emitting the generated photons out of the device and into the far-field (as seen in red). This distinction will be useful in **Ch. 2.3**, when strategies involving the improvement of the EQE of PeLEDs are discussed.

Finally, Luminance (L) is represented in units of cd/m$^2$ and is used to describe the human experience of observing light intensity, which is the main figure of merit when discussing lighting applications that are intended for human experience. To obtain the luminance, the previously determined photon flux needs to be corrected with the photopic function, which describes the specific light response of the human eye.

## 2.2 Metal Halide Perovskites

Various LED emissive materials exist on the market today, including the original III-V semiconductors, organic compounds and even quantum dot-based materials. However, a class of semiconductor material called metal halide perovskites (MHP) has gotten immense attention by researchers in various fields, including for light emission applications. Even though this type of material has been known since the 19$^{th}$ century and its optoelectronic properties have already received some attention in the late 20$^{th}$ century, the research only really took off in the last 2 decades once its promising application in the field of photovoltaics became clear [29]. Since then, it is now being considered as a major contender for the development of future technologies in a variety of fields [17]. In this chapter the properties and advantages of the material class, specifically relevant for the field of light emission and with a special focus on the type of MHP used in this work, will be discussed.

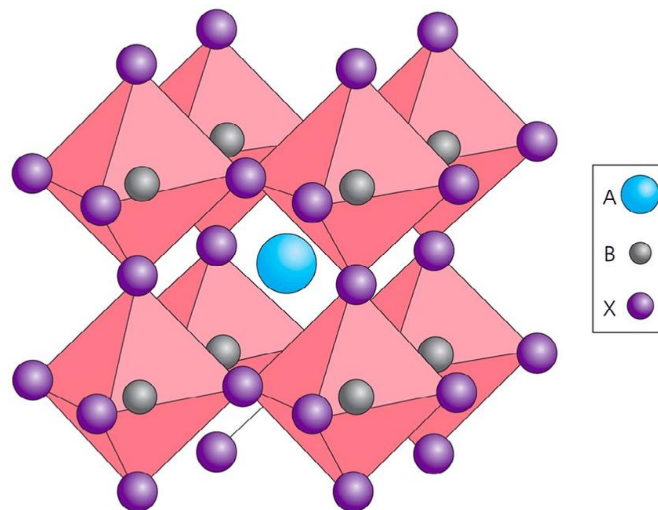


*Figure 2.4: A schematic representation of the perovskite crystal structure. [5]*

The MHP material class is defined by its unique crystal structure, as shown in **Figure 2.4**. Here A represents a monovalent cation (usually either Cesium or a small organic ammonium compound such as methyl ammonium), B a divalent metallic cation (usually Lead or tin) and X a halide anion. The relatively undefined nature of this crystal structure immediately highlights one of its greatest advantages as an immense amount of variation within the material composition is possible. This allows for a large range of properties to be tuned such that the material can be optimized for a variety of applications. For example, by varying the relative composition of halides the bandgap of

the material, and therefore its emission wavelength, can be tuned along a broad colour range as shown in **Figure 2.5** This advantage is made even more relevant by the material's low-cost facile solution-based synthesis protocol, which allows for fast fabrication and therefore feasible investigation of a broad parameter space for rapid device optimization.

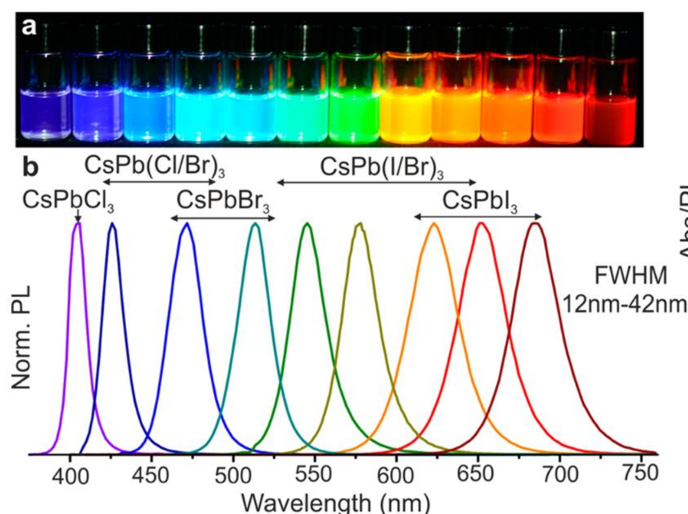


*Figure 2.5: Perovskite nanocrystals exhibit a composition-tunable bandgap over the whole visible spectrum. a) visual observations under a UV-lamp, b) normalized PL measurements [6]*

In addition to varying the stoichiometric ratio of elements present in the crystal, the solution-based synthesis also allows for additional chemicals to be added to the precursor mixture which can have a large effect on the final crystal structure and morphology of the material. For example, the addition of so-called 'linking molecules' can induce the formation of crystal phases with varying dimensionality (n), also called (Quasi-)2D or 2D/3D mixed phase perovskites. An example of perovskite with differing dimensionalities is shown in **Figure 2.6**. Varying the dimensionality of MHPs has been shown to have a substantial effect on various optoelectronic properties such as charge mobility, radiative recombination rates and device stability.

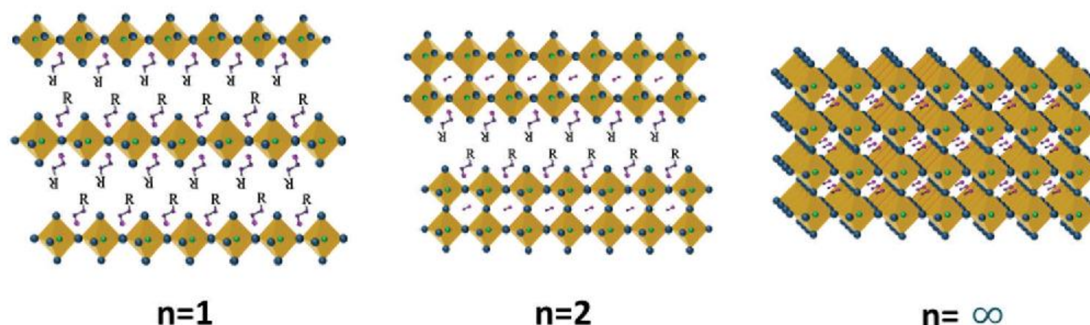


*Figure 2.6: A schematic representation of perovskite crystals of varying dimensionality (n) [7].*

These examples highlight several reasons why this material class is an interesting candidate for the possible integration in many different applications, including light emission technologies. Therefore, the current status of the perovskite LED (PeLED) technology and will be discussed in the next part of this chapter.

### 2.2.1 Perovskite LEDs

The field of perovskite LEDs has, similarly to its photovoltaic counterpart, made significant developments in the last decade. This is not surprising as the general architecture and desired optoelectronic properties are closely related. The fast improvements stem partly from the previously mentioned advantages of the material, but also owe a lot to the developments already made in both thin film LEDs (specifically OLEDs) and perovskite photovoltaics, which both laid the foundations for the high-quality perovskite thin film synthesis and provided an established database of CTL and contact materials and fabrication methods [26].

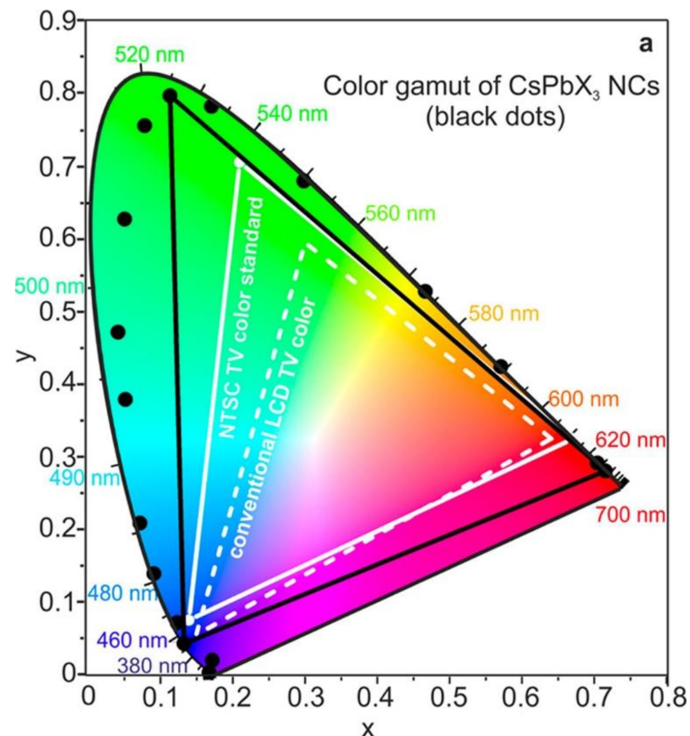


*Figure 2.7: A graph showing CEI chromaticity coordinates of perovskite nanocrystals, compared to other common colour standards [6].*

Furthermore, the HMP material possesses several intrinsic properties which make it especially suitable for lighting and display based applications, such as a high defect tolerance, balanced charge carrier effective masses, good charge mobility and high colour purity (as shown in **Figure 2.7**). All these factors had a hand in achieving the high EQE possible in PeLEDs at this moment, as it has seen a rise from below 1% in the first devices, to above 20% in recent publications [26].

Unfortunately, there are still problems associated with the system. First of all, the PeLEDs are not yet ready for commercial use as the lifetime is generally still far below the 10.000 hours that are required for valid competition in the market. The low stability of the devices is associated with the migration of ions throughout the perovskite and CTLs and is a challenging problem to solve as its dynamic nature makes it difficult to properly characterize [30]. Secondly, the EQE can still be significantly improved as 20% is well below the theoretical maximum as well as below some of the better OLEDs. It is known that most of the losses occur during the outcoupling light, so the main way to improve the overall efficiency is in designing strategies to improve the OCE [9]. As this is the main goal of this project, the next chapter will focus more on this topic.

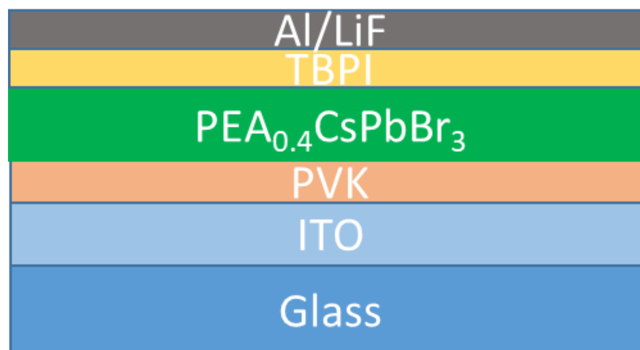


*Figure 2.8: A schematic depiction of the reference PeLED device stack used primarily in this work.*

However, a main outline of the PeLED system utilized in this work will be provided to better interpret the results presented in **Ch. 4**. **Figure 2.8** shows a schematic overview of the reference PeLED device, which will be discussed from the bottom up.

It starts with a transparent glass substrate as a cheap and sturdy bottom surface, on which a pre-deposited layer of Indium Tin Oxide (ITO) is located. This is transparent as well, and acts as the conductive bottom electrode. On top of that is a thin layer of Polyvinylcarbazole (PVK) as a organic polymer HTL, which is again transparent to allow (together with the ITO and glass) for the transmission of emitted light out of the device.

The next layer is the emissive perovskite thin film. More specifically it is Phenylethylammonium Cesium Lead Bromide, which is a quasi-2D perovskite. This means a distribution of various 2D and 3D crystal phases of the perovskite are present, which all have a slightly varying bandgap energy due to a difference in quantum and dielectric confinement. This creates an effective energy funnel in which the high bandgap (low n) states with a higher exciton binding energy transfer the charge carriers towards the low bandgap (high n) states, where they can be efficiently radiatively recombined [8]. This type of perovskite crystal structure can significantly improve the EQE and luminance of device with respect to bulk perovskite. A schematic representation of this mechanism is shown in **Figure 2.9**. It is important to note that an additive molecule (18-crown-6) is used in the perovskite synthesis to promote a good distribution of crystalline phases throughout the film to improve the funnel effect [12].

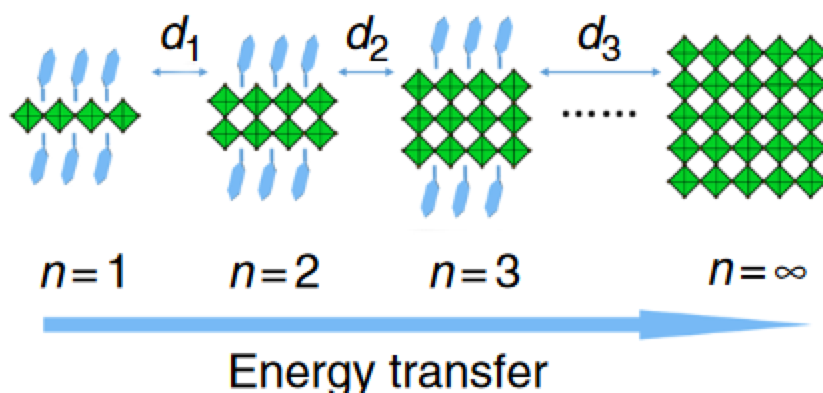


*Figure 2.9: Schematic representation of the energy transfer mechanism of perovskite crystal structures from low dimensionality (n) and large bandgap crystals to high dimensionality and small bandgap crystals [8].*

On top of the perovskite layer, a thin layer of TBPI is deposited which is often used as an ETL due to its electron conductive properties. Then a very thin LiF interlayer is situated on top the ETL. This type of layer was not covered in the standard LED stack discussed before, however it plays an important (although specific) role in the device operation as it initiates the diffusion of lithium and fluoride ions to the top contact and ETL respectively [11]. This lowers the Schottky barrier height and width, which in turn lowers the turn-on voltage and improves both the current density and charge balance of the device.

Finally, on top of the LiF a layer of Aluminium is deposited as a standard top electrode. Most layers of this device stack were chosen because they are often used together in publications [26,30], so the synthesis procedure and characteristics are well known, and it allows for easy comparison of results to the literature. The exception here is the perovskite layer, which was used at Cambridge during the collaboration and had shown to be compatible with the rest of the device stack to produce promising and reliable results. A schematic of the band alignment between the various layers are shown in **Figure 2.10**, which shows that it is generally energy favourable for the electrons and holes to travel to the perovskite layer in this device stack.

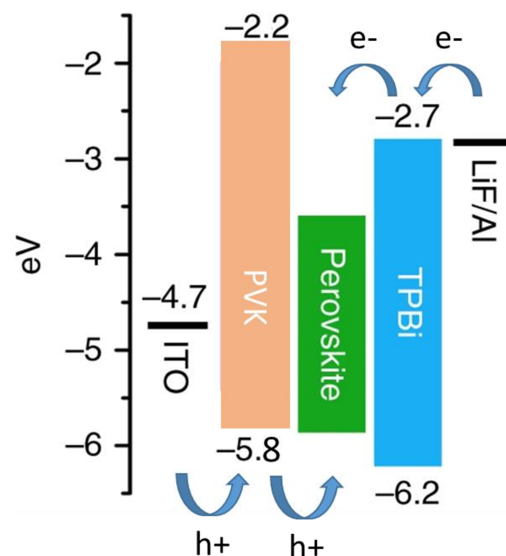


*Figure 2.10: An energy diagram showing the band alignment of the LED device stack, inspired by [8] and added information on energy values from [26]. The difference between various 2D & 3D perovskite crystal phases is not represented in this diagram.*

## 2.3 Light Management in PeLEDs

As mentioned before, the OCE is thought to be the main limiting factor in the EQE of PeLEDs. **Figure 2.11** shows the main loss mechanisms in a typical perovskite bulk LED, depending on the position in the emissive layer where the photons are generated. In these simulations, only a maximum of 25% of the light is actually emitted out of the device, as most of it is lost in so-called 'waveguide modes'.

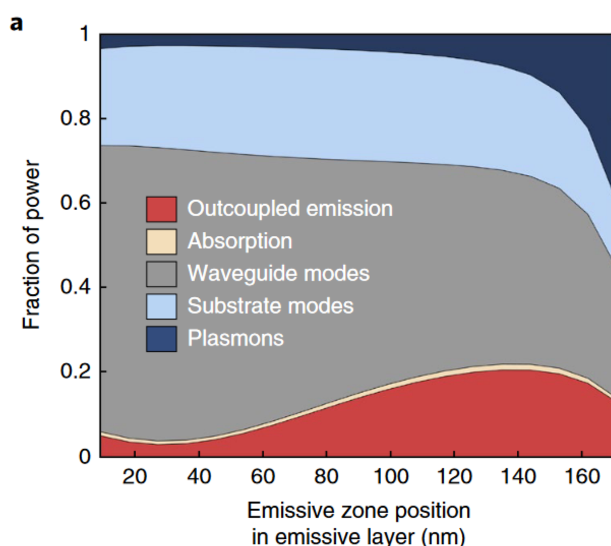


*Figure 2.11: A modelled graph showing the fractional optical power distribution of emitted light in a PeLED as a function of the position in the emissive layer [9].*

In this context, this represents the fraction of light that is trapped within the perovskite layer by Total Internal Reflection (TIR), which is a condition that can arise when there is a large difference in refractive index (n) between a medium and its surroundings. This is due to the fact that light bends when entering a medium with a different n. If this bending is strong enough and the angle of incidence is wide enough it can cause the light to be reflected, effectively trapping the light within the medium until it is re-absorbed or reflected in some other way. This condition is shown in **Figure 2.12** (top). As it happens, perovskite has a relatively high refractive index ($n \approx 2.0$-$2.6$) when compared to typical CTLs ($n \approx 1.6$-$1.8$) [2], especially when in the quasi-2D phase [31]. This means that the generated light only has a limited escape cone around the normal incidence and as photons are usually emitted equally in all directions, a lot of light is lost this way.

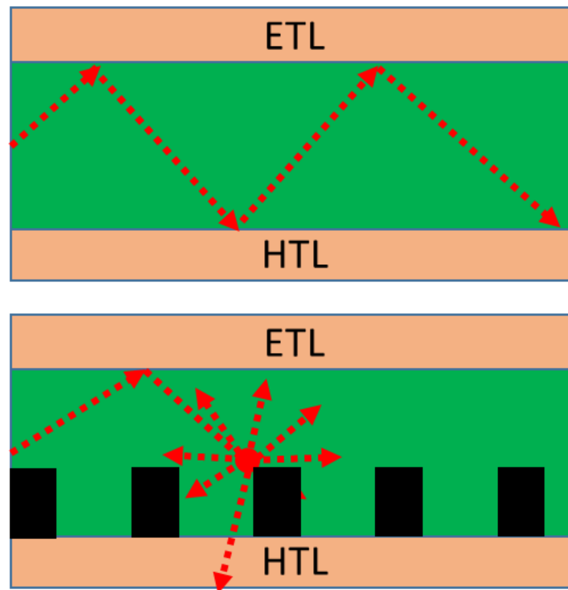


*Figure 2.12: A schematic representation of total internal reflection (TIR) of light within a PeLED (top) and how a nanopattern can induce scattering of this light which allows a fraction of it to still escape the emissive layer (bottom)*

Fortunately, there are ways to mitigate this issue, such as the introduction of a nanopattern (either periodic or random) in the perovskite layer that can reduce the waveguide modes by acting as a diffraction grating, which scatters the light into distinct diffraction orders. This allows the light to get another chance to exit the perovskite medium if it is now located within the escape cone. A schematic of this is shown in **Figure 2.12** (bottom). The advantage of a periodic nanopatterns in comparison to randomly oriented structures is the increase in control over certain properties of the outcoupled light, such as a preference for a certain directionality or possible even polarization, which opens the door to LEDs with designer properties which only depend on the type of nanopattern utilized [2].

Such periodic nanostructures have recently been shown to be able to significantly improve the EQE of PeLEDs and can be manufactured in a variety of ways, both ground-up (CVD) and top-down (Laser ablation) [32]. However, nanoimprinting remains the most common and cost-effective approach, while still achieving high resolution (sub-10 nm) and pattern quality over several $cm^2$ [14]. Yet direct imprinting of the perovskite layer is challenging as (re)crystallization of the film needs to occur during imprinting which can introduce variations in crystal quality. Therefore, a popular approach is to introduce the pattern on the CTL or an interstitial layer below it instead [18-24,28].

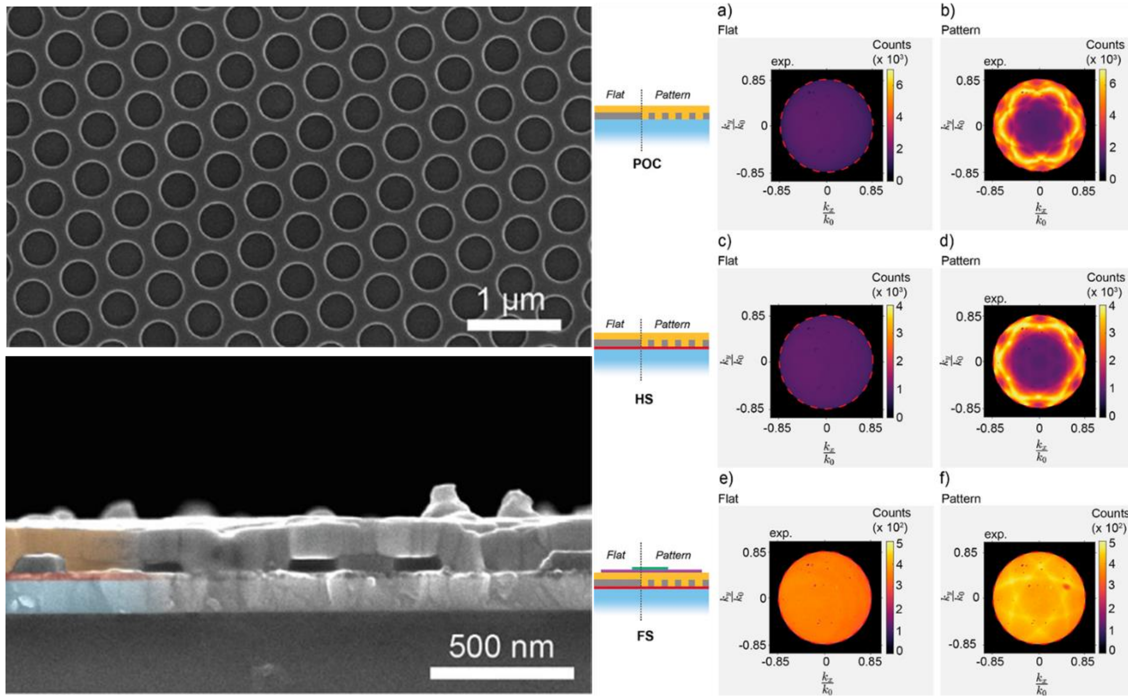


*Figure 2.13: An overview of relevant results obtained by Muscarella and Cordaro et al. which showcases a SEM image of the fabricated nano-hole pattern (top-left), a SEM cross-section of the full device stack (bottom left), and Fourier microscopy images of the patterned and flat reference devices [2].*

However, as far as we are aware, no publication as of yet has attempted to utilize an optically inert and periodic interstitial layer on top of the CTL and thus in direct contact with the perovskite layer to improve its electroluminescent properties except for the publication of Muscarella and Cordaro et al [2], of which this work is a continuation. Here, a silica-based resin layer is patterned in a nano-hole array in between the HTL and perovskite using a specially designed imprinting stamp (see **Ch.3** for details) to improve the OCE and therefore overall luminescence of the device while also inducing an observed directionality of the emitted light (as shown in **Figure 2.13**). Unfortunately, they were not able to produce PeLEDs of significant electroluminescent efficiency in either the patterned and unpatterned stacks, and therefore only conclusions based on the photoluminescent response could be made. Therefore, the goal of this project is to reproduce these results using functional PeLEDs and thus showing improved and directional electroluminescence instead of photoluminescence.

# 3. Experimental Methods

This chapter describes the experimental steps that were performed to acquire the results shown in Chapter 4, which includes the full fabrication of the nanopatterned PeLEDs and the various characterization techniques utilized to study them.

These methods were mainly obtained from previously published results, including the SCIL patterning and general device fabrication [2], and the Perovskite procedure [8,10,12,13]

## 3.1 Chemicals

An overview of chemicals used in this work are listed in *table 3.1*. No further purification steps on chemicals were performed.

*Table 3.1: A full list of Chemicals including substrates, solvents and cleaning agents used in this work.*

| Chemical Substance | Chemical Formula /Abbreviation | Manufacturer | Properties |
|---|---|---|---|
| **Substrate** | | | |
| Japan NSG display glass | Glass | Kintec | Polished grade |
| Indium Tin Oxide | ITO | Kintec | 10-15 Ω/sq, thickness ≈125 nm |
| **Cleaning Agents** | | | |
| Detergent | Decon90 | Decon | |
| Acetone – Analytical Reagent Grade | Acetone | Biosolve | >99.8% |
| Iso-Propyl Alcohol – Analytical Reagent Grade | IPA | Biosolve | >99.8% |
| **Solvents** | | | |
| Chlorobenzene | CB | Sigma Aldrich | >99.8% |
| Dimethyl Sulfoxide | DMSO | Sigma Aldrich | >99.9% |
| **Perovskite Precursors** | | | |
| Cesium Bromide | CsBr | Sigma Aldrich | 99.999%, perovskite grade |
| PhenylethylAmmonium Bromide | PEABr | Greatcellsolar | Purity not listed |
| Lead (II) Bromide (for perovskite precursor) | $PbBr_2$ | TCI | >98.0% |
| Hexaoxacyclooctadecane | 18-crown-6 | Sigma Aldrich | >99.0% |
| **Layers** | | | |
| Polyvinylcarbazole | PVK | Sigma Aldrich | $M_n$ = 25,000 - 50,000 |
| Poly(4-butyltriphenylamine) | Poly-TPD | Sigma Aldrich | $M_w$ > 20,000 g/mol |
| T1100 Nanoglass | Sol-gel | SCIL nanoimprint | |
| Phenylethylammonium Cesium Lead Bromide | $PEA_{0.4}CsPbBr_3$ | Cambridge | |
| 2,2′,2"-(1,3,5-Benzinetriyl)-tris(1-phenyl-1-H-benzimidazole) | TBPI | Ossila | >99.5% |
| Lithium Fluoride | LiF | Sigma Aldrich | >99.98% trace metal basis |
| Aluminium | Al | | Wire form |

## 3.2 PeLED fabrication

This chapter describes the various steps performed for the full device fabrication, including the equipment used. It is structured per layer to give a bottom-up chronological overview of the manufacturing process. The procedure is meant to closely resemble the protocol performed at Cambridge so the final results can be compared to reference devices manufactured there. However, when deviations inevitably do occur the differing procedure as performed in Cambridge will be *highlighted* afterwards.

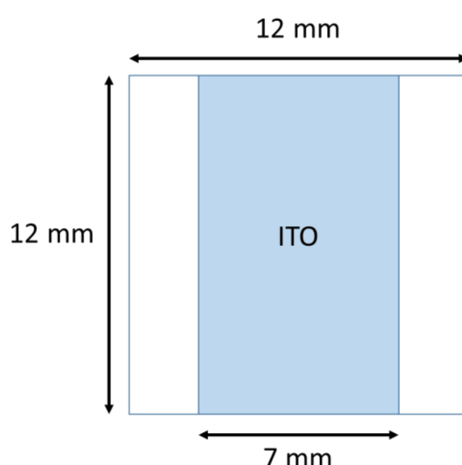


*Figure 3.1: A diagram showing the dimensions of the pre-patterned ITO layer on top of the glass substrate.*

The ITO substrate is prepatterned in a 7x12 mm strip centred on 12x12 mm Japan NSG display glass as shown in **Figure 3.1**, with a $SiO_2$ buffer (≈23 nm) in between the ITO and glass. The ITO thickness is around 125 nm with an RMS roughness 1-2 nm and a sheet resistance of 10-15 ohm/sq [insert Kintec website link].

Before any further fabrication, the ITO substrate is cleaned by a standard cleaning procedure involving scrubbing with detergent in demi-water before washing it by submerging in demi-water, acetone and IPA for 10 minutes each while sonicating in an ultrasonic bath. *In Cambridge, instead of the scrubbing step an additional sonication step with detergent in demi-water is performed prior to other sonication steps.* Afterwards, the substrate is dried by blowing with a nitrogen gun before exposing it to a low intensity oxygen plasma for 16 minutes in a Diener Electronic Zepto Plasma Cleaner to remove any remaining solvents and oxidize the ITO surface to ensure a better wetting of the PVK layer. *Cambridge instead uses a Nano Bio Analytics UVC-1014 UV-Ozone cleaner for 30 minutes.* The substrates were then quickly transferred to a nitrogen atmosphere glovebox to prevent material degradation (typical $O_2$ level < 10 ppm, $H_2O$ level < 1 ppm) and start the PVK depositing procedure.

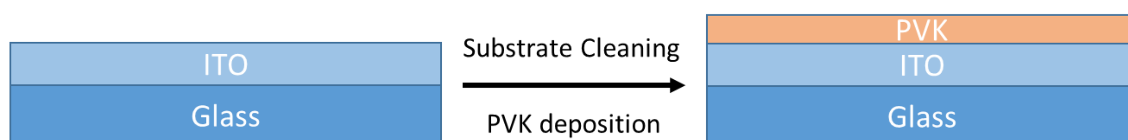


*Figure 3.2: A sideview layer diagram representing the ITO cleaning and PVK deposition procedure.*

The PVK precursor solution was made by dissolving PVK in Chlorobenzene (between 5-15 mg/mL, but typically 15 mg/mL) while stirring at room temperature until all visible solid material was dissolved (usually within 15 minutes). No further filtering is required. A fresh batch of PVK precursor was made every few weeks to prevent deterioration over time.

Once the PVK solution was ready, the ITO substrate was mounted on the spin-coater and cleaned again by a nitrogen gun to ensure no dust or other small particles resided on the sample. 45 µL of freshly stirred PVK solution was then drop-casted on the sample to ensure a full wetting of the surface & the spin-coating was quickly started to obtain a uniform layer coating. 2 different PVK spin-coating protocols were used throughout this project. The parameters for each were: 1. 2000 rpm for 45s, Acceleration = 1000 rpm/s & 2. 4000 rpm for 30s, Acceleration = 2000 rpm/s, which were developed at AMOLF [2] and Cambridge [?] respectively. Directly afterwards, independent of the spin-coating protocol, the substrate was annealed at 140$^{o}$C for 20 minutes on a heating plate to remove excess solvent and allow for proper crystallization. After PVK layer deposition, samples were stored under $N_2$ atmosphere until the SCIL procedure could be started.

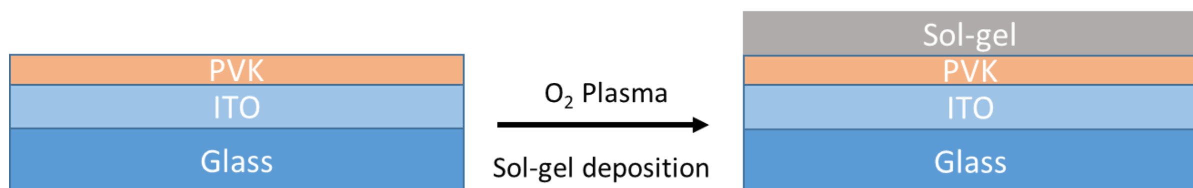


*Figure 3.3: A sideview layer diagram representing the $O_2$ Plasma treatment and Sol-gel deposition procedure.*

*As the nanopatterns were only manufactured at AMOLF, this section concerning SCIL was not performed in Cambridge*. Samples were transferred from the glovebox into an ISO 7 Cleanroom where the SCIL procedure was performed, to prevent the contamination with dust and other small particles. The samples were first subjected to $O_2$ plasma (25 sccm at $10^{-6}$ mTorr) for 30s in an Oxford Instrument's PlasmaPro 80 to improve the adhesion of the sol-gel to the substrate. The sol-gel was removed from its refrigerated storage at least 30 minutes before spin-coating to heat to room temperature. This was done to prevent premature evaporation of the solvents during curation. The sample was then mounted on the spincoater and cleaned one final time with a nitrogen gun. 2-3 drops of sol-gel solution were then drop-casted on the sample through a 0.2 micron filter to prevent any small particles that might have entered the solution during handling to be transferred to the substrate, and the spincoating procedure was started (2000 rpm for 8s, acceleration = 2000 rpm/s).

Before detailing the next step in the SCIL procedure, the specially manufactured stamp should be highlighted (see **Figure 3.4**). This stamp contains both flexible (high Young modulus) and rigid (low Young modulus) PDMS deposited on a thin glass substrate. This allows for the stamp to combine the advantages of rigid imprinting (good resolution & low pattern distortions) and soft imprinting (long stamp lifetime). Furthermore, the thin glass is flexible in the out-of-plane direction, which allows the stamp to conform to inhomogeneous surface conditions [14].

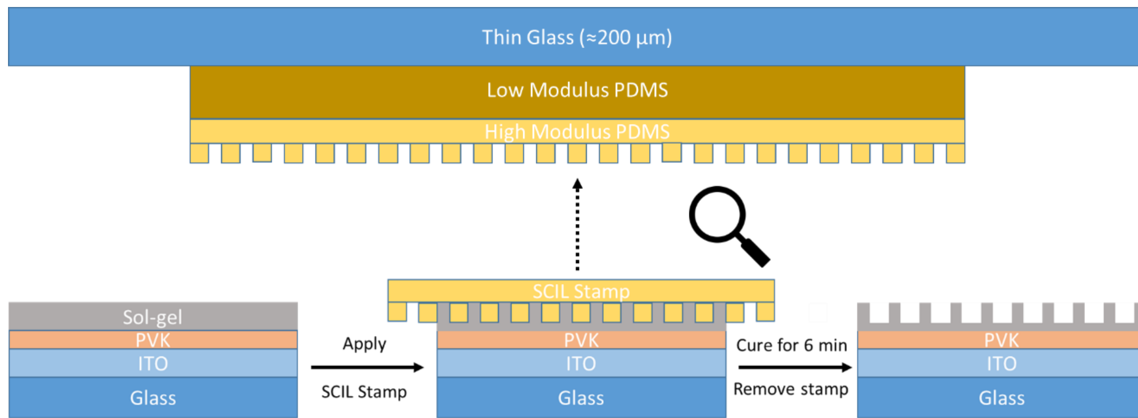


*Figure 3.4: A sideview layer diagram representing the SCIL stamping procedure, including an overview of the SCIL stamp.*

After sol-gel deposition, the sample was then placed on a stable platform and the SCIL stamp was carefully positioned such that the patterned area fully covers the substrate. Light pressure was uniformly applied to the stamp to ensure good contact between the pattern and the substrate and then left to cure for 6 minutes to let the sol-gel dry and form a hardened silica material before carefully removing the sample using a pair of tweezers. All actions after the sol-gel drop casting until applying the stamp were performed in rapid succession to limit the premature hardening of the sol-gel as much as possible. Finally, the patterned substrates were subjected to another plasma treatment in the Plasma80 ($CHF_3$ & Ar, both 25 sccm at $10^{-6}$ mTorr) to remove the silica in between the imprinted features. This was necessary to expose the PVK, as a good contact between HTL and perovskite is needed to facilitate charge carrier transport.

After the SCIL procedure, the stamp can be cleaned by water and ethanol, or by performing the stamping procedure on an empty silica wafer to remove aggregations on the stamp.

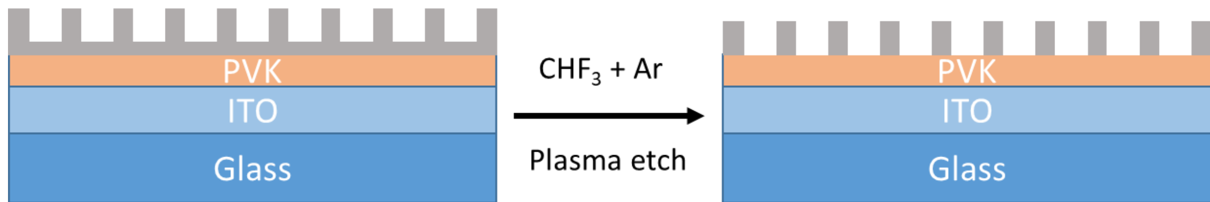


*Figure 3.5: A sideview layer diagram representing the sol-gel etch procedure.*

The samples are now ready to be transferred to Cambridge, where the rest of the fabrication process will occur. To ensure a safe transport, the sample boxes were sealed in 3 layers of sealing bags under nitrogen atmosphere. Once in Cambridge, they were again transferred to a nitrogen-filled glovebox before opening.

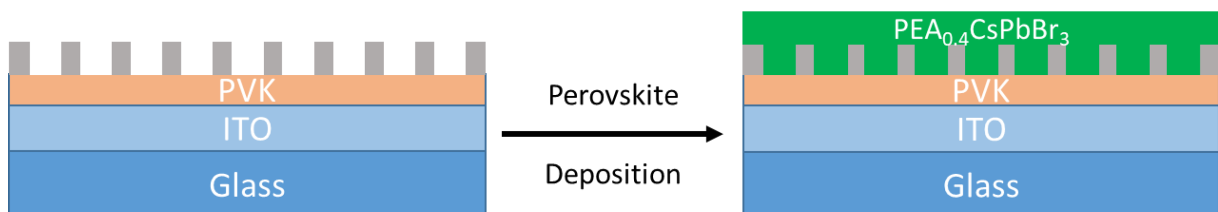


*Figure 3.6: A sideview layer diagram representing the perovskite deposition procedure.*

The perovskite ($PEA_{0.4}CsPbBr_3$) precursor solution was made by adding 89,4 mg of CsBr, 32,3 mg of PEABr, 146,8 mg of $PbBr_2$ & 9 mg of 18-crown-6 to 2 mL of DMSO. To fully dissolve the material the solution was heated to 60$^oC$ while stirring for at least 2 hours, after which no solid material should be present. Before spin-coating, the precursor was cooled down back to room temperature in 10 minutes by removing the heating source. The nano-patterned substrates were additionally subjected to UV-ozone for 60 seconds to improve the wetting of the precursor solution. This was not necessary for unpatterned samples as PVK adequately wetted the precursor solution without. Once the samples were mounted on the spin-coater, they were again cleaned using a nitrogen gun before 55 μL of precursor solution was drop-casted & the spin-coating procedure was started (Speed = 1000 rpm for 5s, then 4000 rpm for 55s, Acceleration = 1000 rpm/s). Samples were then immediately annealed for 10 minutes at 90$^oC$ on a heating plate, to remove excess solvent and allow for proper crystallization of the perovskite.

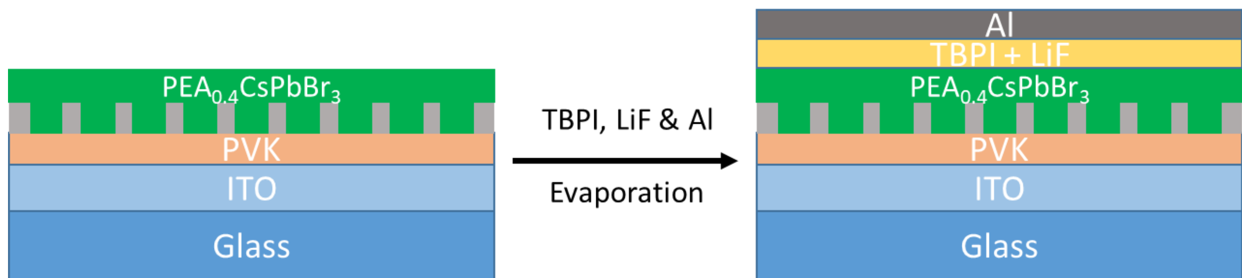


*Figure 3.7: A sideview layer diagram representing the ETL, interlayer and top-contact evaporation procedure.*

The samples were then transferred to a Mbraun PROvap Thermal Evaporator to deposit the ETL & top contact layers using a standard recipe. First 40 nm of TBPI acting as an ETL was evaporated over the full substrate at a rate of 0.1 A/s, followed by a thin interlayer (5 nm) of LiF at a rate of 0.05 A/s, which is known to improve the turn-on voltage, current density and charge balance of PeLEDs [18].

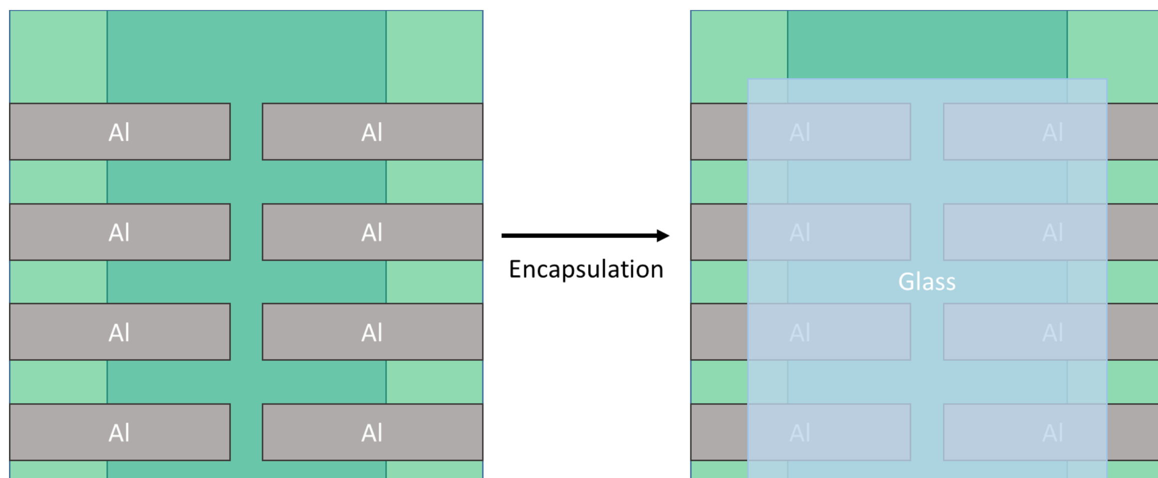


*Figure 3.8: A schematic top view of the patterned aluminium top contact and the encapsulation procedure.*

A patterned Al layer (100 nm) as top contact consisting of 8 pixels with a surface of 4.5 $mm^2$ each was evaporated on top of the LiF using an evaporation mask. A schematic top view of this pattern is shown in **Figure 3.8** (left) including the underlying ITO layer to highlight the overlap area which defines the actual pixel area. Some space is left unpatterned at the top to leave room to connect the bottom contact. The first 5 nm was deposited at 0.1 A/s, the second 5 nm at 0.5 A/s and the rest (90 nm) at 1 A/s. This was done to ensure a good quality Al coating at the interface, while the quality of top part is less important and as such can be deposited at a faster rate to save time.

Finally, the samples were encapsulated (as shown in **Figure 3.8,** right) by gluing a piece of glass with UV-adhesive that can be cured in seconds when exposed to UV-light, so they can be transferred outside the nitrogen environment without immediate deterioration of the perovskite. However, as the sides and top were still partly exposed due to the need of connecting the device to a circuit in the future, the layers will still be exposed to some air or moisture and thus should be kept to a minimum by minimizing the time outside the glovebox.

*Figure 3.9: A sideview layer diagram representing the alternate device architecture fabrication process.*

Towards the end of the project some variations to standard layer ordering were explored, specifically the placement of the sol-gel layer in between the ITO & PVK layer. This required some minor variations from the protocol, apart from switching the order of the PVK spincoating and SCIL procedure, which will be highlighted here. First off, the $O_2$ plasma treatment time before the SCIL procedure was increased to 2-5 minutes as the sol-gel solution did not seem to wet the ITO layer as well as the PVK. As ITO is more stable towards various plasma treatments when compared to PVK, this should not significantly affect the morphology or performance of the layer [33]. However, the longer plasma treatment did not seem to significantly increase the wetting either, so in the future this can probably be neglected. Secondly, the concentration of the PVK precursor solution was lowered to 5 mg/mL to prevent the formation of aggregated PVK hotspots and encourage the local deposition within the nano-holes.

## 3.3 PeLED & Layer Characterization

This chapter describes the characterization techniques utilized to obtain the data shown in **Ch. 4**, which concern both the individual layers of the device as well as the full device performance. The techniques mentioned include AFM, Profilometry, SEM, Photoluminescence spectroscopy and EQE measurements.

Atomic Force Microscopy (AFM) measurements were performed to analyse the surface morphology and thickness of select layers in high resolution. Thickness determination was done by scratching a surface using sharp metal tweezers to expose the underlying substrate and performing a linescan between the scratched and unscratched surface to determine the layer thickness from the observed step height. 2 different AFM setups were used, Bruker Dimension Icon & Fastscan respectively, depending on their availability. However, the setups are very comparable and should provide similar results. Measurements were done in Peakforce mode using ScanAsyst software to optimize the scanning parameters during measurements. Typically a ScanAsyst-air tip was used as it is the

standard tip to use for measurements done in air in ScanAsyst mode. Both Gwyddion and Nanoscope-analysis software were used to analyse and correct the obtained data.

Profilometry is principle very similar to AFM, as it also allows for the height and morphology of a surface to be determined. The main difference is that it provides lower resolution (especially in the lateral dimensions) but is significantly faster and easier to use. Therefore, it was utilized instead of AFM when a high resolution was not required and results were needed quickly or a large quantity of samples needed to be investigated. The measurements were performed on a KLA Tencor Stylus Profiler P7, with an applied force of 2 mg.

Another way to obtain information on a system's surface characteristics is with Scanning Electron Microscopy (SEM) as, in contrast to transmission-based electron microscopy, this technique detects the secondary electrons that are emitted by the atoms close to the surface of the material under investigation and therefore provides certain topographic information which typically differs from the more direct scanning probe techniques. The main advantage of the technique in this work is it allows for a much larger area to be studied in significantly less time, while still providing comparable resolution to AFM when the scanning area is decreased. Furthermore, it allows for cross-sectional observations of the stacked layers, which provides unique information on the vertical layer dimensions that cannot be easily obtained from AFM. However, these cross-sectional measurements can be more time intensive and usually provide less resolution. SEM measurements were performed on a FEI Verios 460, at a beam voltage of 5 Kilovolt and a beam current of 100 Pico Ampere. Cleaved samples were achieved by locking the samples in a specially designed sample holder before scratching the samples using a diamond scribe and separating the 2 sides using a plastic hammer. The cross-sectional measurements were then performed using a tilted sample holder and movement stage, allowing for a tilting angle up to $90^{o}$. Images were analysed by Fiji ImageJ software.

To investigate the electroluminescent (EL) properties of the devices, a home build JVL measurement setup at Cambridge was utilized. This allows for a variety of optoelectronic parameters to be determined while performing a voltage sweep on individual pixels of the device. The main quantities of interest for this work are the Voltage (V), radiated luminance ($cd/m^2$), current density ($mA/cm^2$) & EQE (%). The setup uses a Keithley 2400 sourcemeter to measure the current density and voltage and a calibrated silicon photodiode detector at a known distance (2.5 cm) to quantify the photon flux. From these, the total luminance values can be derived based on the emission function of the PeLED and the known spectral response of the detector. The EQE is then calculated by assuming the LED exhibits a Lambertian emission profile.

Finally, the photoluminescent (PL) properties of the device are investigated using a WITec microscope system, which allows for PL measurements at known locations on the sample due to its integrated microscopy setup. PL signal in contrast to EL is generated by exciting the system with a laser to generate charge carriers instead of applying a bias voltage. The system utilizes a Thorlabs Fabry-Perot Benchtop laser source (405 nm) in combination with an Acton SP-300i spectrometer. The data is analysed using Project FIVE software.

# 4. Results & Discussion

This chapter discussed the achieved results which were acquired by the previously described methods in **Ch. 3**. It has been organized per layer of the device, describing the fabrication optimization and at the end the results concerning the full device will be discussed. Finally, attempts to improve the previously mentioned device architecture will be shown.

## 4.1 Layer Fabrication Optimization & Characterization

To fabricate a functioning device a lot of optimization is required due to the inherent specifications that the system needs to adhere to, which are usually strongly dependent on the specific conditions used during fabrication and therefore slight variations in these conditions can significantly affect the eventual performance of the device. It is therefore critical to keep a strict eye on the state of each layer that is fabricated, and thus an attempt to provide a full overview of each step of the device manufacturing will be given.

### 4.1.1 The Bottom Contact

As the starting substrate already has its ITO layer pre-deposited by the substrate manufacturer, the amount of optimization that can be done is limited. However, it is still important to know what characteristics the layer has to help identify or dismiss possible problems that might occur during the further fabrication process and to verify some of the properties specified by the manufacturer to ensure proper quality of the substrate. A specific property that is important for our goals is the roughness of the surface, as a very thin layer of PVK has to cover the ITO and the extremes of the depths & heights can influence the lower limit of the PVK-layer thickness that can be used while still fully covering the ITO (as shown in **Figure 4.1**.) The main action performed on the ITO layer except for the standard solvent sonication cleaning procedure is a O2 plasma treatment step which is used to oxidize the layer to improve PVK wetting during spin-coating that has been shown to improve its layer quality [34].

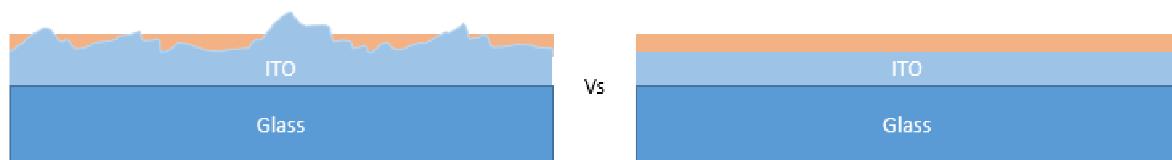


*Figure 4.1: A sideview layer diagram representing the different results from spin-coating the PVK layer on top of the ITO, depending on the ITO roughness.*

To that end, the bare ITO layer was investigated using AFM shown in **Figure 4.2**, which show representative results of ITO before (left) and after (right) it was subjected to the plasma cleaning procedure. AFM is the prime technique for this purpose, as it can very accurately determine the morphology of a surface on the few nm scale. The results show a surface covered with a comparable distribution of grains of varying sizes (100-1000 nm) which are occasionally separated by thin (≈50 nm) and deep (5-15nm relative to surrounding surface) line defects. The exact origin of these lines is unclear but, as they already occur continuously over the whole ITO surface before plasma cleaning, it is assumed to be an intrinsic property of the layer left by the depositing process and thus not something that can be easily counteracted.

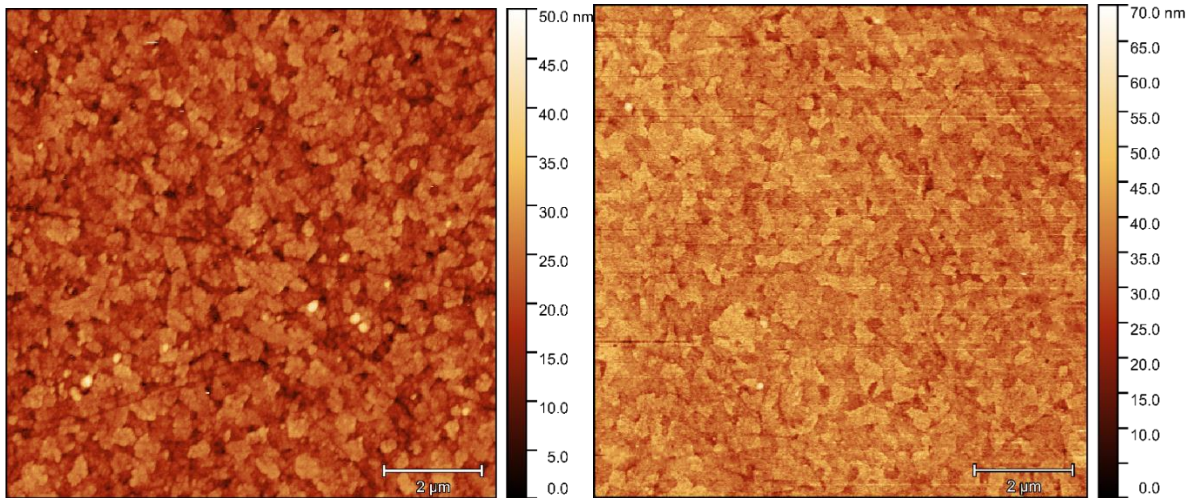


*Figure 4.2: Topographic AFM images of unetched (left) and etched (right) ITO.*

There is a slight difference between the ITO layer before and after plasma treatment. Namely, after plasma treatment the ITO Root Mean Square (RMS) roughness increases by about 1 nm (from 4-5 to 5-6 nm), which indicates a larger average variation in the height of the surface. This is also represented in the AFM image as a larger total height gradient (50 vs 70 nm), which largely originates from an increase in depth of the trenches in between the grains as the majority of the surface is situated at a relatively higher heights (≈35 vs 20 nm), which is clearly visible from the color gradient. This is most likely caused by the O2 plasma inhomogeneously removing a small amount of either ITO or contamination from the surface. These RMS values differ significantly from the values given by the manufacturer (1-2 nm) and suggest that the ITO surface might either not be as resistant the performed cleaning procedures as previously thought or the surface was contaminated in some way before the measurements (assuming the specifications of the manufacturer were true). However, it is unclear how significant this increase of average roughness of 1 nm will be in the final device but as long as the PVK layer thickness is significantly larger than this RMS value it should at least be able to fully cover the ITO layer. Furthermore, Cambridge has shown even greater RMS roughness values in the ITO layer in their AFM measurements and seeing as the devices obtained from those substrates still give adequate luminescent qualities, it is assumed to not be a significant limiting factor.

### 4.1.2 The HTL Layer

The first layer that is added to the cleaned ITO substrate is the HTL (PVK) conform the standard layout of an LED as described beforehand. This layer together with the ETL described later will facilitate the transport of charge carriers to the perovskite emission layer and is therefore crucial in achieving the maximum IQE by allowing for a fast hole transport and keeping a good balance of charge carriers in the perovskite material. It is difficult to determine these qualities without fabricating and testing full devices, but it is known that a full and homogeneous coverage of the metal contact is needed while keeping the layer itself as thin as feasibly possible to make sure the holes are not limited by the hole mobility of the layer [35]. It is also paramount that the PVK will retain its quality and coverage after 2 distinct plasma etching steps which are necessary for the SCIL procedure. Therefore, initially an investigation by AFM is again in order as it allows for the morphological features to be investigated similar to the ITO layer as described before. These results are shown in **Figure 4.3.**

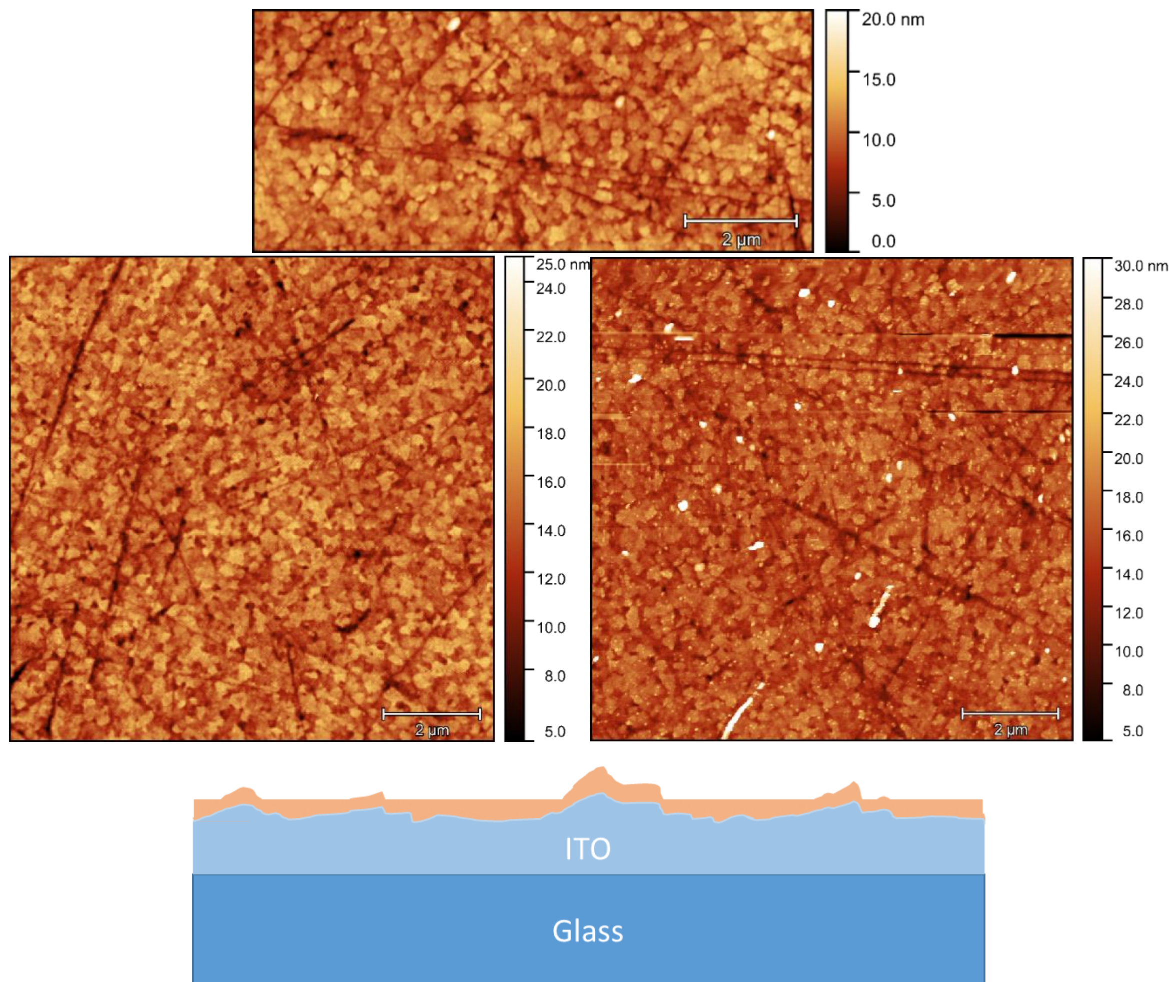


*Figure 4.3: Topographic AFM images of unetched (top), $O_2$ plasma treated (left) and Ar+$CHF_3$ plasma treated (right) PVK, and a sideview layer diagram representing the current device architecture.*

The PVK AFM results in **4.3** (unetched, O2 plasma & sol-gel etch treatment respectively) look very similar to previously shown ITO AFM results with the surface consisting of a distribution of grains and line defects. However, although the line defects are very similar to ones observed in ITO the grain size distribution is significantly smaller, usually a few 100 nm. Furthermore, the RMS roughness of the surfaces is significantly reduced (≈ 2 nm) which often corresponds with a smaller grainsize indicating a more homogeneous coverage then the underlying ITO layer**.** As indicated by the RMS roughness, the surfaces are very similar as is also visually apparent in the AFM images. It is important to note that the scaling of the images has been altered to highlight their similarities, as they do not necessarily align in the original data (See **Figure A.1 in Appendix)**. That is because the unetched image contains a low concentration of small high spots that are not present in the etched image (possibly because it is a contamination that would be etched away by the O2 plasma treatment) that shifts its relative surface down in the color gradient.

While the etched measurement contains a single line which is significantly deeper than the others (which could be caused by the O2 plasma treatment similar to the ITO), that shifts its relative surface upward. If these effects are corrected for, the images appear very similar in structure and height distribution. The same can be said for the sol-gel etched case, although both effects are happening at once and in a more pronounced way, as there are small areas of significantly increased height (100 nm) as well as measurement defects of low height. If these are both corrected for again a similar surface image is obtained with a similar RMS roughness (as long as the high peaks are

excluded for the calculation). It is important to mention that the significant increase in local high spots could be a consequence of the etch procedure, but it is more likely a result from a scratching procedure as described below. All in all the results indicate that both the O2 plasma & sol-gel etch treatment do not significantly affect the surface morphology of the PVK layer on the µm scale, although this does not show that the optical properties are unaffected as well.

Additionally, to verify the thickness of the PVK layer SPM techniques (both AFM and profilometer) can again be utilized by additionally employing a local layer removal method, in which a small part of the PVK is scratched away using metal tweezers to expose the underlying ITO. By finding this scratch and measuring the difference in height between the 2 layers, the PVK layer thickness can be determined. The difference between the AFM and profilometer in this regard is that the profilometer is significantly faster and more straightforward in use but its resolution (mostly lateral but also vertical) is worse when compared to AFM. Thus usually, the profilometer is utilized first in the initial stages of optimization when a broad parameter range is investigated which results in many samples that need to be measured, while the layer thickness is expected to be high enough to adequately resolve. However, as the HTL layer needs to be as thin as possible while still withstanding the plasma treatment procedures & maintaining full coverage [35], eventually AFM is employed to acquire more reliable and high-resolution data of the thinner films. A representation of these AFM measurements is given in **Figure 4.4**, while the data obtained from the profilometer during layer optimization can be found in **Table A.1 in Appendix**.

The large AFM overview scans in **4.4** (left) clearly show a difference between the scratched and unscratched region, both in relative height and texture. Furthermore the scratched region is relatively flat which is a good indication that the ITO has been successfully reached as it is more robust to mechanical stress than the polymer HTL layer and thus allows us to determine an accurate thickness profile of the PVK layer. A significant difference in relative height between unetched and O2 etched samples can be derived from the linescans shown in **4.4** (right), from 20-25 nm for the unetched layer to 10-15 nm for the etched layer. This result is a little surprising as it is mentioned in [2] that this plasma treatment should remove ≈5nm of PVK. This could indicate some difference between our PVK layer compared to the publication that could arise from the varied spin-coating protocol or highlight a slight inaccuracy in the publication, which is understandable as a significantly thicker PVK layer was used and thus less need for accuracy in determining the precise thickness. Nonetheless, it is important to keep in mind for any future protocol optimization. The above images also represent results from the final optimized PVK layer protocol and will be used for all subsequent results unless otherwise specified. The final PVK thickness (10-15 nm) was chosen to ensure sufficient coverage of the ITO layer as it is significantly higher than the RMS roughness of the underlying layer (5-6 nm).

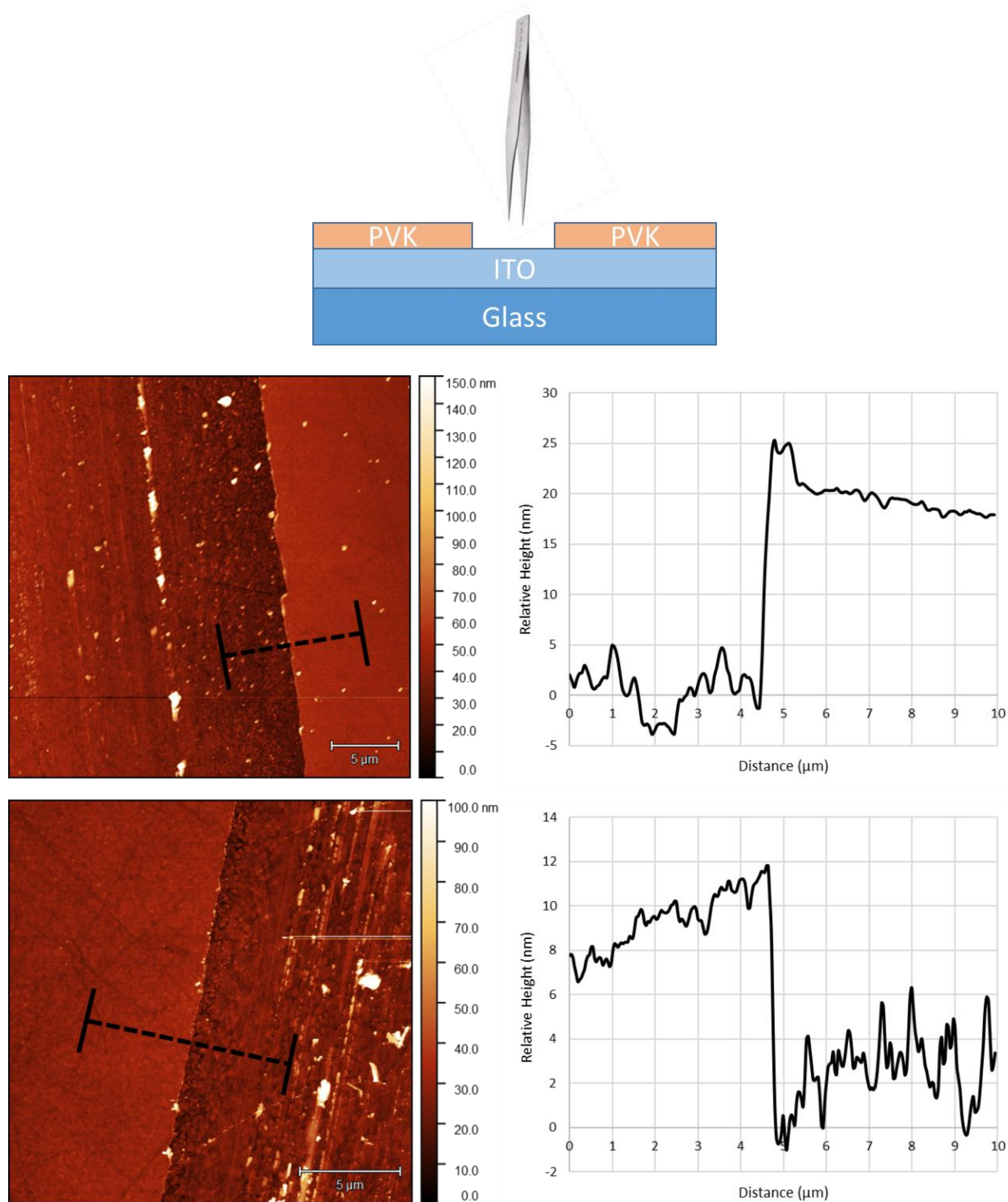


*Figure 4.4: A sideview layer diagram representing the current device architecture (top) and topographic AFM images of unetched (top left) and $O_2$ plasma treated (bottom left) surfaces including linescan positions, the data of which is represented on the right.*

As these AFM measurements are done on a more disordered system in comparison to the previously discussed results, it is expected that a few more complications may arise during measurements and in the final images. Some significant examples relevant for the images shown are highlighted here to validate the results discussed above. Firstly, increased levels of local high spots in both layers (but more significantly in ITO) are observed. These can be attributed to the defects & contamination that arises by using such a crude layer removal strategy as these in homogeneities gradually decrease in frequency the further away from the scratch is measured and were not observed before the scratch was made. Another defect originating from the scratching procedure is a slight accumulation of matter observed at the etch of the scratch interface, which is clearly observed in **4.4** (top right) as an

additional bump in the linescan after the initial layer edge is reached. This bump is therefore not taken into account when determining the PVK layer thickness. Finally, a slight decrease (≈5 nm) in height of the PVK layer over several μm is observed in the linescans. This could be a result from the scratching operation as well by similarly pushing PVK away from the scratch, but it is unlikely for such a crude method to lead to a smooth decrease in height while keeping the rest of the surface relatively uniform. It is more likely to originate from a slight variation in the overall substrate height as this is probably not constant in the few nm range or an artifact from the AFM as it can be difficult to keep such height measurements constant over many μms and as the system under investigation is more disordered this can be more difficult to correct for in post processing.

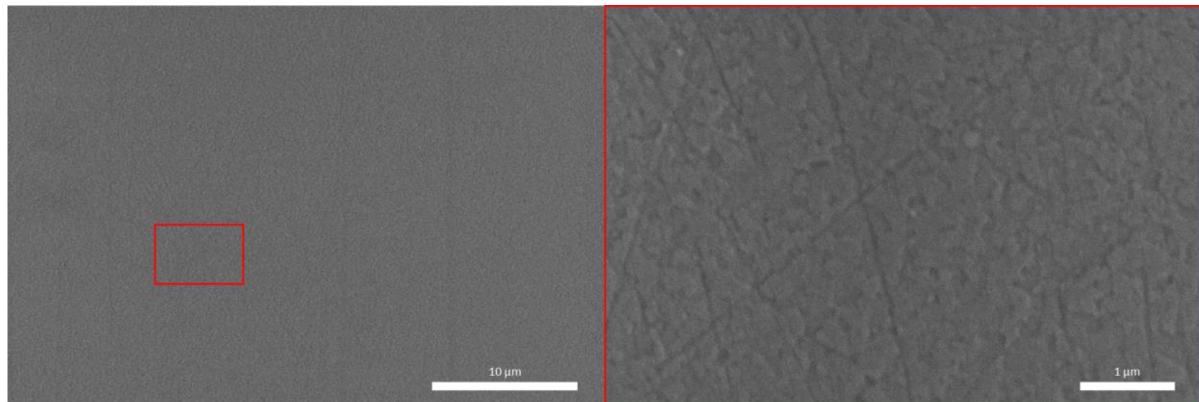


*Figure 4.5: Topographic SEM images of etched PVK, showing a large overview area (left) with a zoomed in area marked by a red rectangle, which is shown in on the right.*

Finally, the etched layer was also characterized by SEM as it can also resolve some morphological features to correlate with the AFM results but more importantly it is much more time efficient for investigating large areas which makes it feasible to determine if the PVK fully covers the whole ITO layer on the substrate. A typical representation of the SEM results are shown in **Figure 4.5,** a large overview area (left) and zoomed in area (right) respectively. The large overview shows that the PVK layer has fully covered the glass & ITO substrate in the area under investigation, as the zoomed in area highlights a similar morphology as observed in the AFM images and can thus be assumed to be PVK. By imaging several of these large areas at different points on the substrate, it can be concluded that a (relatively) clean and fully-covering PVK layer has been achieved. This is also validated by optical observations by eye which shows a slight uniform orange coloring of the substrate.

All in all, it is concluded that even though the obtained PVK layer from the optimized protocol is not perfect and could possibly be further improved in terms of uniformity, the resulting thickness and total coverage is sufficient for the purpose of this research

### 4.1.3 The Sol-gel Layer

After the HTL, it is time to discuss what is probably the most interesting layer for the topic of this research. Namely, the nanopatterned sol-gel layer that will ultimately define the maximum light outcoupling improvement and directional emission of said light. To this end the pattern/layer dimensions and quality (on both long and short scale) are critical, as the first property that will determine how the material is expected to interact with the generated light & the perovskite material on the local scale, while the second will determine how well it will achieve this both locally and in the far field by looking at the amount of defects observed in the pattern. To keep things simple, the procedure is kept as close as possible to the protocol initially described in [2] as this will allow us to make certain assumptions on how the light outcoupling and directionality is expected to behave. Furthermore, general pattern dimensions and quality can more easily be verified by comparing to previously published results. These will coincidentally also be the first characteristics under investigation, using techniques previously introduced to study the ITO & PVK layer (SEM & AFM).

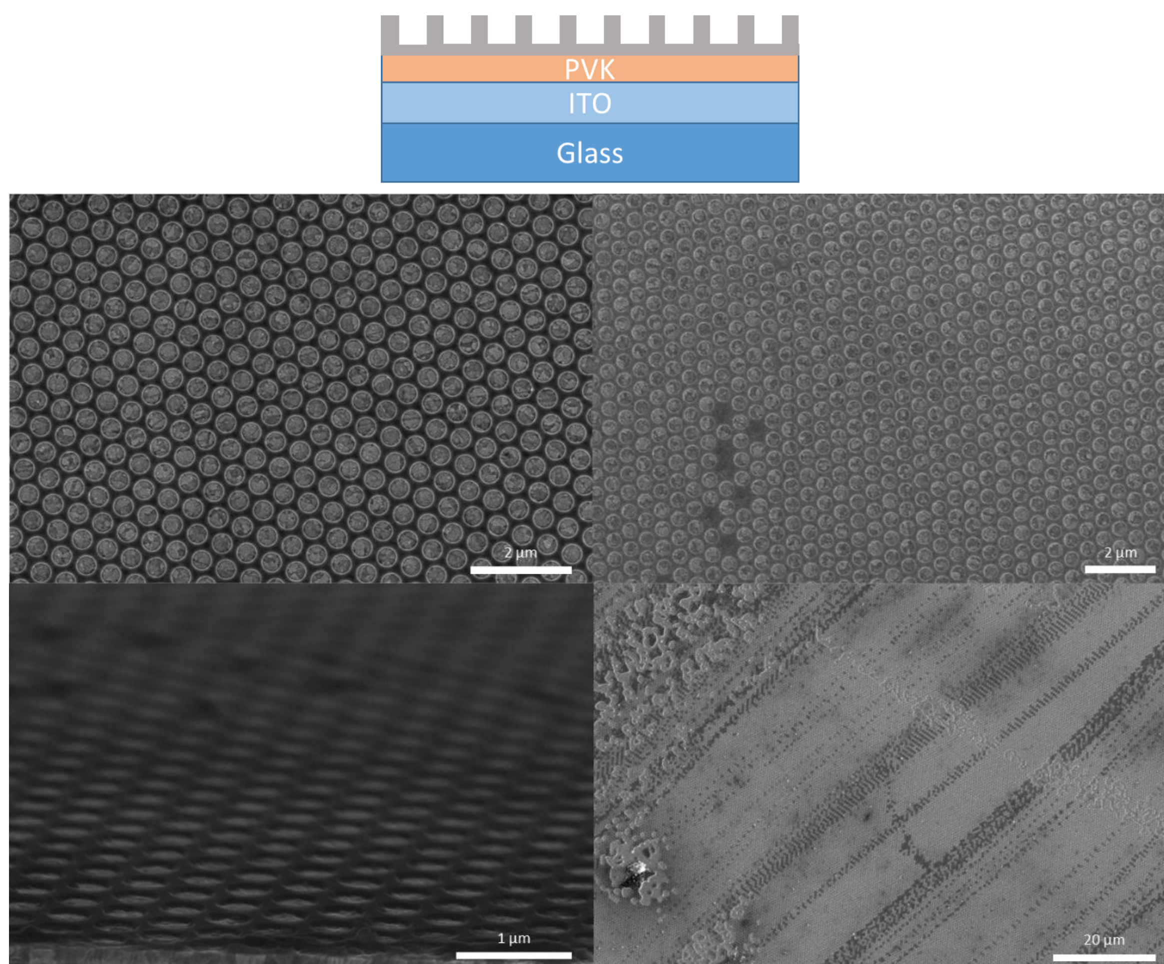


*Figure 4.6: A sideview layer diagram representing the current device architecture (top) and top view topographic SEM images of the unetched (top left), etched (top right) and without preceding $O_2$ plasma etch (bottom right). A sideview image at $75^o$ (bottom left) is included to better show the hole-pattern.*

**Figure 4.6** shows representative SEM results of the sol-gel layer before (top left) & after (top right, bottom left) sol-gel etch procedure, and without performing O2 descum plasma treatment before SCIL procedure (bottom right). From these, the lateral dimensions can easily be verified as the borders between the sol-gel and underlying material are clearly distinguishable by the difference in contrast and are confirmed to be in agreement with the known stamp pattern and previously published results [2] (with a variation of a few nms, which are expected as the resolution of the SCIL technique is only ≈ 10 nm but are assumed negligible in the grand scheme of things). It can also be verified that the sol-gel etch procedure does not affect these lateral dimensions (at least within the degree of accuracy of the measurements). The side view (75$^{o}$) (bottom left) also confirms that the holes themselves are intact and gives a better perspective on how the layer actually looks like.

Some defects are observed in both etched and unetched samples in the form of (partly) missing holes in the array and varied contrast within the holes themselves. The first originates from defects already present in the SCIL stamp and are thus directly transferred to the sol-gel pattern, or from irregularities in the stamping procedure cause by the human factor as the stamping is done manually by hand. It is unclear exactly what is the cause in these smaller defect sites as they are hard to reproduce due to the difficulty in finding them on the substrate. However, these small defect sites are an insignificant percentage (<1%) of the total pattern coverage, and are therefore assumed to be insignificant in their effect on the final light outcoupling. The second type of defect is observed as a significant difference in contrast within the holes themselves. These do not originate from any clear inhomogeneities in the morphology of the surface at the bottom of these holes, as seen in the AFM measurements in **Figure 4.10**. Therefore they probably stem from an artifact in the SEM measurement caused by a difference in electron conductivity of the underlying surfaces and do not reflect any characteristics of the sol-gel pattern itself. This is further backed up by the observation that line-defects similar to the ones observed in the PVK/ITO layers can also be distinguished throughout the hole-array.

Due to the previously described concerns with the effect of the O2 descum protocol on the PVK layer quality, an attempt was made to perform the SCIL procedure without a preparative O2 etch, the results of which are shown in **4.6** (bottom right). It should be immediately clear that the resulting sol-gel pattern is of lesser quality than the previously shown patterns, as the surface is riddled with hole defects and even aggregations of large sol-gel masses which would probably severely limit the conductivity and therefore proper functioning within the full device. It is thus assumed that the O2 plasma treatment step is necessary in the current protocol to ensure good sol-gel adhesion to the surface needed for proper SCIL patterning.

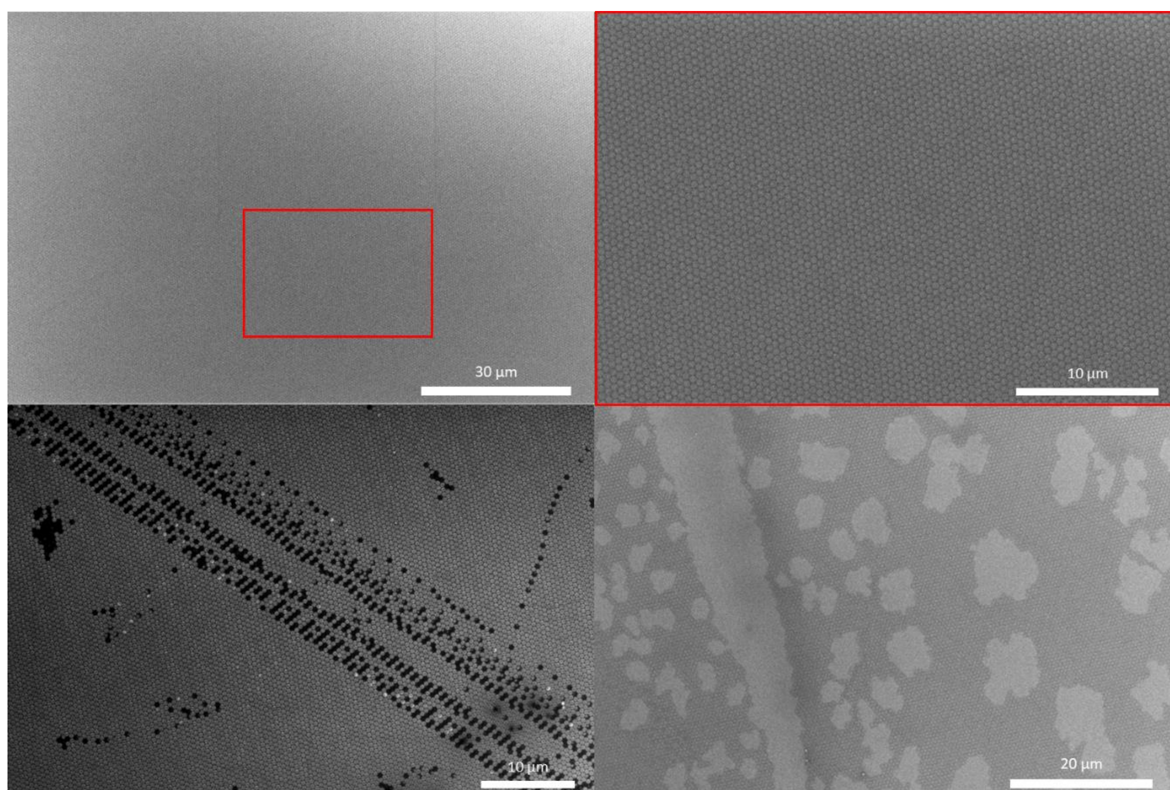


*Figure 4.7: Topographic SEM images of various observed sol-gel patterns. The top-left image includes a red rectangle which highlights the area of the top-right image.*

Above it was mentioned that the small defect sites only comprise of an insignificant percentage of patterned surface. This description was carefully chosen as it circumvents the main issue observed in SEM images on the large- scale (>50 µm), namely the existence of large defect areas and significant parts of the surface without any pattern present at all (examples of these are shown in **Figure 4.7,** bottom left and right respectively). This does not mean that the whole surface is riddled with these types of defects. The large-scale quality of the pattern varies significantly over the surface, as some areas display an almost perfectly defect-free pattern as shown in **4.7** (top left and right). This again insinuates a problem with either the stamp or the patterning procedure.

To exclude the effect of the age of the stamp and the defects that can originate from subsequent usage, a new stamp with the same pattern dimensions was commissioned. From this point onward the 2 stamps are distinguished by the terms “old” vs “new”. Initially this new stamp seemed to have resolved the issue as SEM results mainly consisted of images similar to **4.7** (top right), however upon closer inspection of the substrates by eye it became clear the patterning was not as universally uniform as initially assumed (shown in **Figure 4.8**). Here a silicon wafer is patterned to show the full 25x25 mm SCIL area which. when observed under the right angle, should result in a square area of constant contrast that displays the characteristic diffraction properties resulting in a rainbow-like light gradient. However, both SCIL patterns show distinctive large-scale deformities in the diffraction square, which differ significantly between each other but can be roughly reproduced over consecutive stamping procedures. This insinuates some problem with the stamps themselves, as they should be identical but deliver consistently different results while the rest of the procedure is kept constant. Curiously the new stamp, which would be expected to be in more pristine condition, delivers less total patterned coverage over the full square when compared to the old stamp. The running theory is that some residual sol-gel got stuck to the SCIL stamp, as this is known to happen from time to time if the adhesion of the sol-gel to the surface is not strong enough. Several attempts

were made to clean the stamp, unfortunately none of them succeeded in improving the resulting patterning.

When the patterned samples are investigated more thoroughly in the SEM, the observations made by eye are reaffirmed as shown in **4.7** (bottom right), where large areas of unpatterned surface are mixed with the patterned background. The reason this was not spotted in the initial SEM investigation is the fact that these large, un-patterned areas can be difficult to properly image as they provide minimum contrast when compared to the patterned areas and are therefore easily dismissed as some error in the focusing of the microscope. This might lead to the conclusion that the old stamp provides a better nanohole-pattern than the new stamp, as more total surface is patterned. However, the old stamp also shows a significantly higher concentration of defects sites on the small-scale, as represented in **4.7** (bottom left), which was also one of the reasons for the new stamp to be commissioned in the first place. Therefore, the importance of higher average long-range periodicity vs short-range defect-free patterning needs to be considered to make an educated assessment. Unfortunately, due to time constraints it was not possible to do a thorough investigation into this matter.

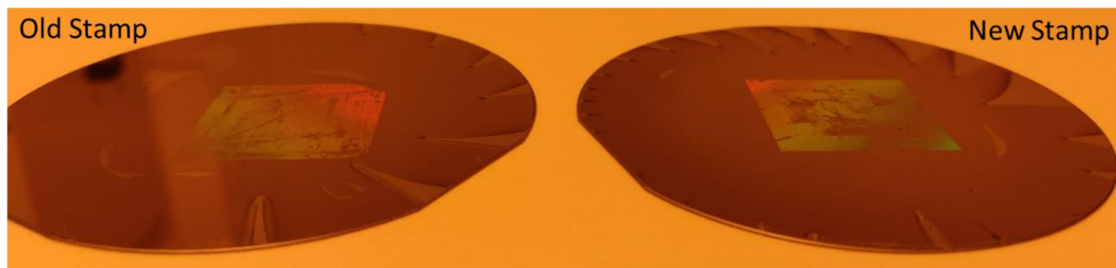


*Figure 4.8: A picture of 2 silica wafers stamped using the "old" (left) and "new" (right) stamp. The observed squares highlight the patterned areas.*

Even though the patterning uniformity is far from perfect, further investigation into the vertical dimension of the layer is still in order to confirm the holes that are present are of the right depth and that no residual sol-gel is present at the bottom of these holes. To this end, cross-sectional SEM is performed in which a substrate is cleaved before imaging from the side at a $90^{o}$ tilt. While this can be a challenging technique to perform due to the necessity of a very sharp cleavage and the difficulty of accurately imaging a tilted surface due to the necessity of properly focusing the electron detector, it can give a unique insight on the vertical structure of a layered structure. The results are shown in **Figure 4.9**, which include a schematic representation of the system under investigation (top) and patterned sol-gel samples before (left) and after sol-gel etch treatment (right) respectively.

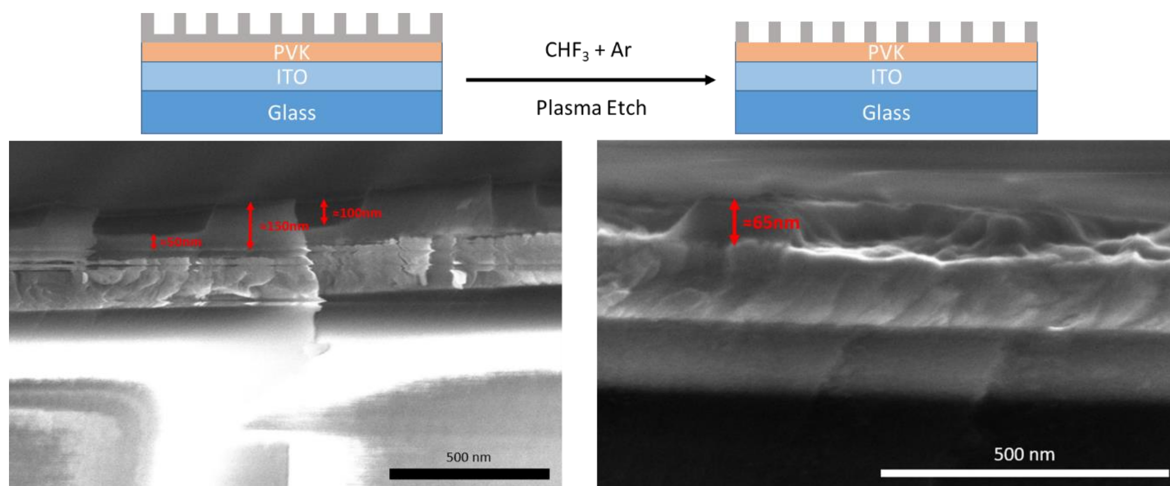


*Figure 4.9: A sideview layer diagram representing the current device architecture (top) and side view topographic SEM images of the unetched (left), etched (right) sol-gel patterns.*

The first apparent artifact in these SEM images is the fact that the bottom glass substrate looks distorted, with some irregular high contrast patterns that can sometimes light up brightly (**4.9**, left). These are called "charging effects" and are caused by electrons hitting a (poorly conductive) material that is being imaged that cannot dissipate the electrons well and therefore ends up accumulating at the surface and effectively charging it up and causing various distortions during the measurement. As glass is an insulating material, these effects are expected but can make accurate measurements difficult. Luckily the ITO layer is quite thick (≈120-160 nm) and can therefore easily be distinguished, however due to the aforementioned artifacts accurate determination of the thickness is complicated. The PVK layer is even more intricate to observe due to its low thickness, however as this has already been determined by AFM in **Ch. 4.1.2** this is not a big issue.

More importantly, the sol-gel layer is clearly distinguishable in both images with less distortions (possibly mitigated by the ITO layer in between) and can therefore provide rough estimates of the vertical layer dimensions as shown in the figures, which correspond to the previously published results and serve as a sanity check for following AFM measurements. Lateral dimensions cannot be extracted from these images, as it is unknown at which point relative to the hole matrix the cleavage occurs. However, the main advantage of this technique is that it allows for the residual sol-gel thickness at the bottom of the holes to be determined, as there is a clear distinction between the sol-gel and ITO morphology, and therefore make sure that all of it is removed during the sol-gel etch process. When comparing the figures, a layer of around 50 nm of sol-gel can be clearly observed in between the nano-holes before plasma treatment, while no such layer is seen afterwards. Furthermore, the depth of the holes is also significantly reduced which, assuming the etch rate is roughly equal over the whole surface, is a good indication that all residual sol-gel is removed. A final observation is that the hole surface appears to have significantly increased in roughness. Whether this is caused by the plasma treatment, or the cleaving procedure cannot be concluded from these measurements, which is another reason further AFM measurements are in order as no cleavage is needed to investigate the surface.

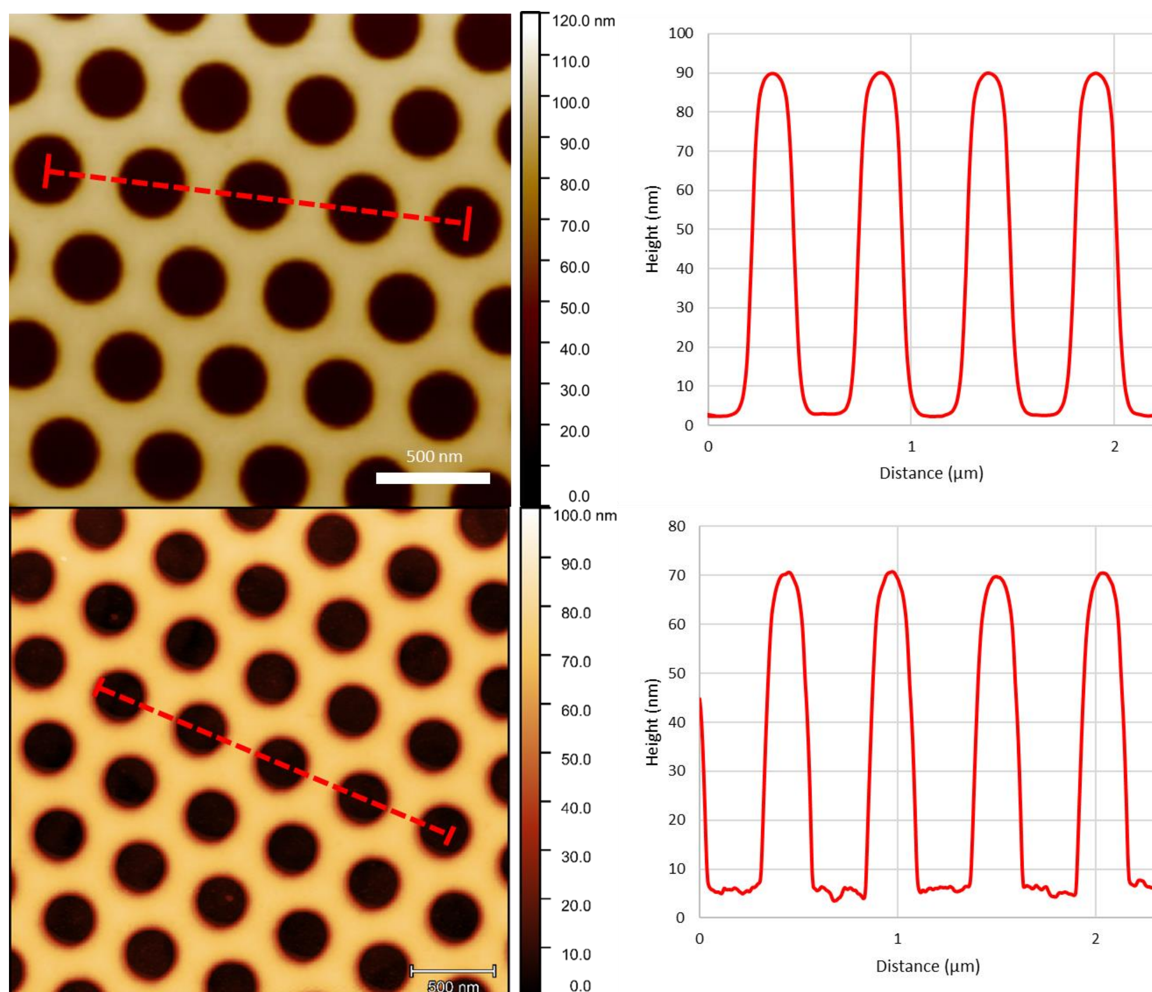


*Figure 4.10: Topographic AFM images of unetched (top left) and etched (bottom left) sol-gel patterns including linescan positions, the data of which is represented on the right.*

AFM measurements of the (un)etched nano-pattern with corresponding height profile linescans are shown in **Figure 4.10**. It is important to mention that these 2 images were acquired on 2 different AFM setups which resulted in a disparity in the data output, which is the reason why the color scaling and general layout of the images varies somewhat. Nonetheless, in both images a clear nano-hole pattern conform to previous SEM measurements (**4.6**) is observed. The edges of the nano-holes are cleanly resolved, which is known to be an issue sometimes depending on the tip and hole dimensions and the surface and height of both the holes and the sol-gel top layer appear uniform. When comparing the linescans before and after plasma treatment, the depth of the holes drops from ≈ 90 to 65 nm which roughly corresponds to the dimensions measured by SEM. Here the AFM values represent a more accurate result due to the specific conditions of the measurements. Interestingly, an increased roughness on the hole bottom surface (RMS≈ 1 vs 2-3 nm) is also clearly observed in the linescans as in the SEM results (**4.9,** right) albeit at a decreased scale. However, as the roughness is comparable to the previously measured RMS of the PVK layer it is likely that this is just an indication that the residual sol-gel has successfully been removed and the PVK layer effectively exposed.

All in all, it is concluded that the sol-gel layer has successfully been manufactured on the local scale, with a high-quality hole pattern of accurate dimensions showing little defect sites and a uniform top and bottom surface on and in between the hole-array before and after the plasma etch procedure.

Additionally, what appears to be a successfully exposed and intact PVK layer with unaffected roughness after plasma treatment is observed. However, long-range homogeneous full-substrate patterning has still not been achieved. The precise reason is thus far unknown, but it is assumed that the SCIL stamps used are part of the problem as significantly different patterns are obtained when varying stamps. It is likely the stamps have suffered some impairment either by direct damage to the pattern, or by aggregation of sol-gel on the pattern. The causes for this can be numerous, but the origin likely lies in some misuse of the pattern during the procedure or, in the case of the old stamp, excessive usage over time might be a factor as well. In any case, continuing the project with a fresh stamp would be the most facile next step to rule out any pre-existing damage or aggregation. While the patterns can also be cleaned, an HF step is likely needed which might further damage the stamp. Sadly, due to time constraints this was beyond the scope of this project and the device manufacturing was continued as planned while keeping these limitations in mind.

### 4.1.4 The Perovskite, ETL & Top Contact Layers

Now that a somewhat satisfactory nano-patterned layer has been achieved, it is time to finish the full LED to try and investigate the optical properties of the device. As this work was performed at Cambridge University using a previously optimized procedure and the time there was limited, the focus was not initially to further optimize the process. Therefore, not a lot of time was spent in investigating the individual layers as the focus lay more on investigating the full-device performance that will be discussed in the next chapter. Nevertheless, during manufacturing a small problem was encountered that needed a slight change in the standard procedure which will be discussed here.

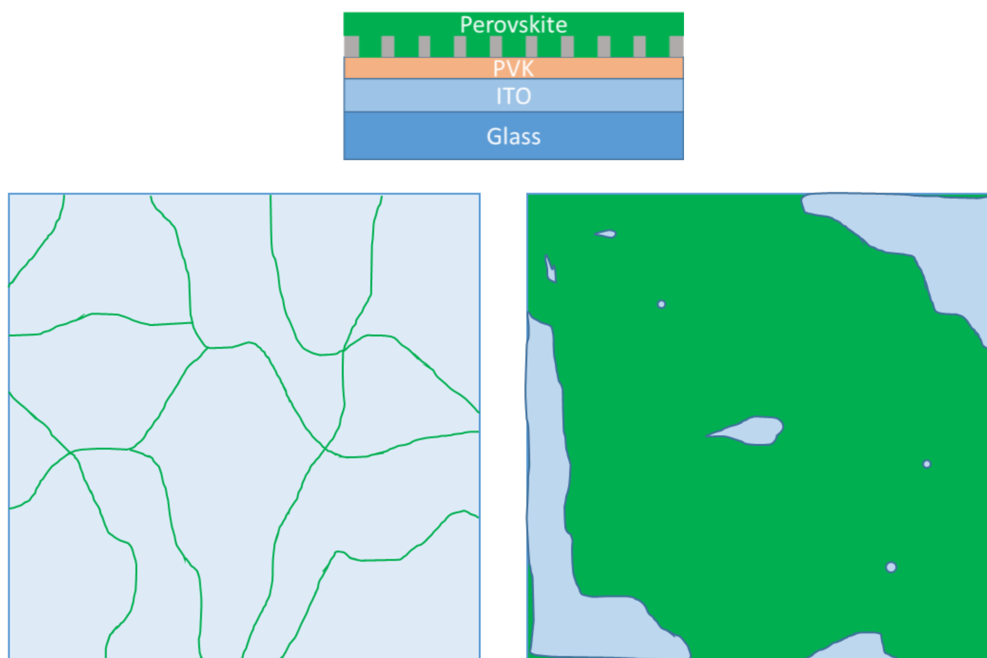


*Figure 4.11: A sideview layer diagram representing the current device architecture (top) and schematic representations of the visual observations after spin-coating perovskites on patterned surface without (left) and with plasma treatment (right).*

Initially, after spin-coating the perovskite-mixture on the nano-patterned substrates, the perovskite did not seem to form the expected crystalline thin film layer but instead randomly oriented thin green lines were observed, as shown in **Figure 4.11** (bottom left) as a schematic representation. These observations were done by eye while exposing the substrates to a low intensity UV-flashlight which will highlight the PL areas. This will give a rough indication of where the perovskite has properly crystallized. It was assumed that the perovskite-solution was not properly wetting the substrate (which was observed during spin-coating) due to the hydrophobic nature of the sol-gel.

Therefore, a short UV-Ozone plasma treatment was performed to oxidize the substrate surface and thus increasing the wettability of the perovskite solution. This significantly improved the final perovskite coverage, although a uniform PL over the surface was not achieved. **Figure 4.10 (**right) shows a schematic representation of a typical surface coverage, with large areas of mostly homogeneous PL but also large areas where no PL was observed at all. A low-resolution photo of the substrates is also included in **Figure A.2** in the Appendix. Curiously, these areas roughly correspond to the successfully patterned areas of the substrate (observed by eye before spin-coating). This seems to indicate a preference of the perovskite to locate within or around the nano-holes, which could allow for a more facile perovskite spin-coating procedure in the future. However, as this is not the topic of this project, it is left for other researchers to possibly investigate. For now, the perovskite coverage was deemed adequate as the main limitation seemed to be the inhomogeneous sol-gel patterning.

The rest of the LED manufacturing process (evaporating the ETL & top contact before encapsulating the device with glass & UV-glue) proceeded as planned (as shown in **Figure 4.12**), with no further alterations to the standard procedure. Therefore, the device was now ready for proper optoelectronic characterization.

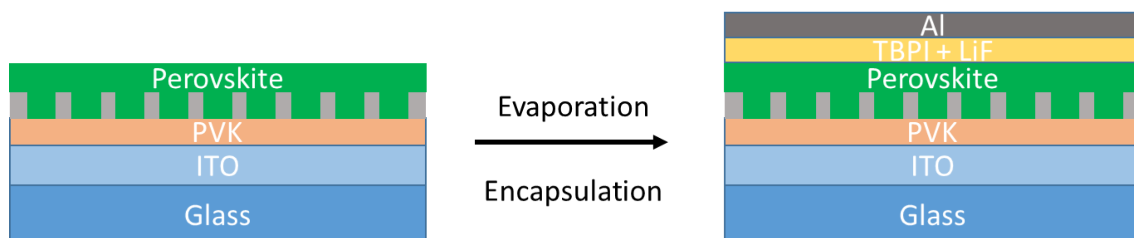


*Figure 4.12: A sideview layer diagram representing the current device architecture*

## 4.2 Device Performance

This chapter will deal with the optoelectronics characteristics of the full stack LEDs (fabricated as described in **Ch. 4.1**). This is the main result from this project, as the end goal was to improve the performance of the devices by the insertion of the nanopatterned sol-gel layer. Unfortunately, due to time constraints accrued during the fabrication process and unfavorably timed equipment failure/maintenance only a small number of devices could be investigated. These measurements are separated into 2 batches, from this point denoted as Batch 1 & Batch 2.

Generally, the most important characteristic of an LED is its electroluminescent properties as these represent the final function that the device will need to fulfill, namely the generation and outcoupling of light under a bias voltage. Within this category, a lot of information and parameters are contained (current density/efficiency, EQE, total luminance, etc.). However, a focus will be made

on the total luminance output as it makes for easy comparison between samples and clearly highlights the main problems encountered in the project. **Figure 4.13** shows a representation of EL results obtained from the full devices with the luminance over voltage data from Batch 1 (top left), a Cambridge reference (top right), an unpatterned reference (bottom left) & the final patterned device (bottom right) respectively. As will be immediately apparent, a lot of differentiations can be made between the various graphs.

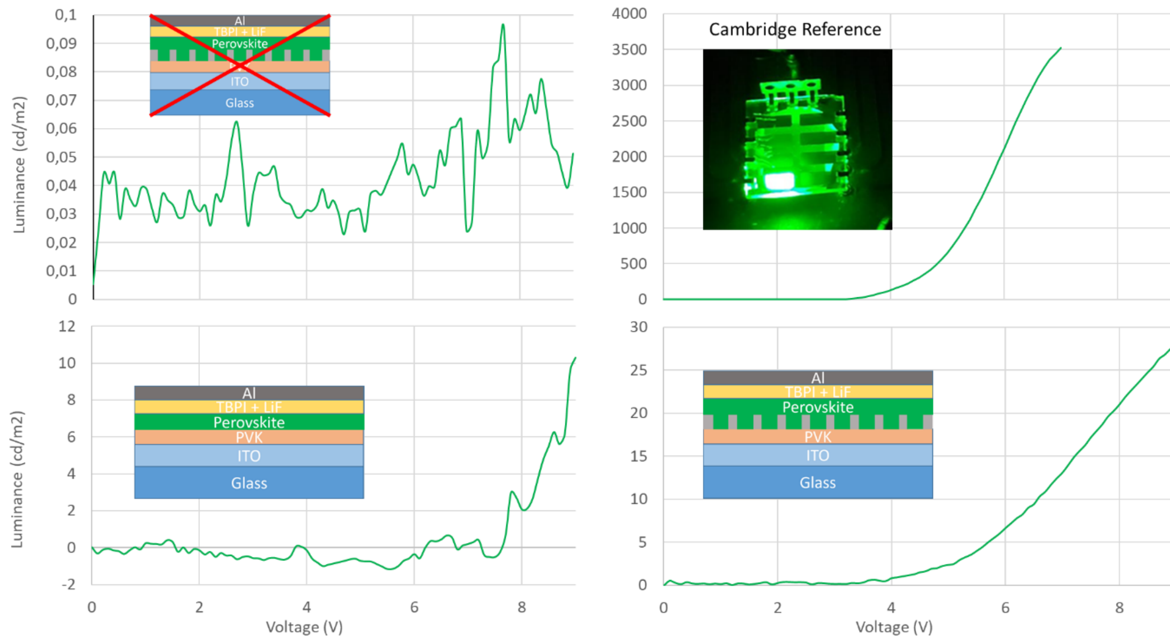


*Figure 4.13: Luminescence (cd/m²) over applied bias voltage PeLED devices. Top left: failed pixel, Top right: Cambridge reference device, Bottom left: unpatterned device, & Bottom right: patterned device.*

First off, individual pixels will not always successfully light up, leading to no significant luminance being observed at all over the whole voltage range as shown in **4.13** (top left). This is expected, as the requirements for a working pixel are quite strict and local variations in the layer quality can severely limit the pixel performance. However, no pixel measured in any of the samples of Batch 1 showed any observable luminance, even though this batch also contained some reference devices which were fully fabricated in Cambridge and whose performance is known and reproducible. Therefore, it was concluded that something went wrong during either the perovskite layer development or during the ETL/top contact evaporation step, however it is unknown what exactly caused the malfunctioning.

To further investigate this hypothesis the PL properties of this device batch were studied (shown in **Figure 4.14**), which can provide more information on the emissive qualities of the perovskite layer, in this case the emission wavelength, intensity and short-term stability over time. The figure depicts a light emission distribution peak around the expected wavelength (≈ 515 nm) with a relatively low intensity but a good stability in the timeframe of the measurement (≈ 5 min). Keeping in mind that the devices were already quite old during the measurements, the low intensity is not very surprising. The good emission stability and wavelength give an indication that the perovskite crystallization was successful and thus probably not the limiting factor in the device fabrication. This is good to keep in mind for future batches as the perovskite deposition on a non-uniform surface can also lead to complications. In any case, Batch 1 was still concluded to be a failure even if the perovskite layer seems to be in good condition.

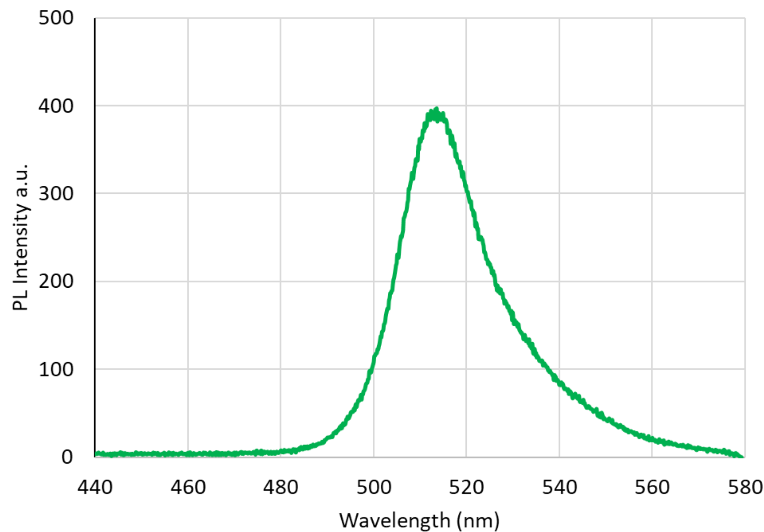


*Figure 4.14: Photoluminescence over wavelength of Batch 1 PeLED*

Luckily, even though the problem with Batch 1 is still unknown it seemed to have resolved itself as Batch 2 shows results more in line with expectations (**4.13**). Here, the Cambridge reference device (top right) exhibits the steep S-shape in the luminance curve, which is characteristic for well-functioning LEDs, with a turn-on voltage around 3.5V and a luminance of 3500 cd/m$^2$ (which is still relatively low when compared to some previously manufactured devices). However, the devices partly fabricated at AMOLF (bottom left and right) do not fare as well as they display luminescence values of about 2 orders of magnitude lower and with either a significantly higher turn-on voltage (around 7.5V in the unpatterned samples) or a more gradual increase in luminescence leading to a maximum luminescence at a much higher voltage point (mainly in the patterned samples). This indicates that something is not as it should be.

While it might appear that the patterned device is outperforming the unpatterned counterpart, the data shown here is from a champion pixel that significantly outperforms its peers with other working pixels exhibiting comparable max luminance to the unpatterned pixels. Furthermore, the pixels on the patterned samples have a lower success rate of actually turning on (37 vs 50%) which probably stems from the inhomogeneous patterning discussed in **Ch. 4.1.3** as this would lead to large parts of the pixel being covered by an insulating sol-gel layer. Even so, the fact that the best performing pixel is from a patterned sample could be a sign that if the substrate is properly patterned, the luminance significantly improves. However, there is not enough data to support such a claim.

It is also important to keep in mind that the only difference between the unpatterned sample and the Cambridge reference is that the PVK layer has been deposited at AMOLF and subjected to O2 plasma treatment. Therefore, it stands to reason that at least part of the problem lies in the quality of the PVK layer. This is not completely unexpected, as the PVK coated substrates need to withstand several days in non-ideal circumstances while being transported to Cambridge and while they are sealed in $N_2$ atmosphere with several layers of containers it is possible that some air might leak into it and affect the samples in some way. This would also translate to the patterned substrates, as the SCIL patterning procedure is performed in air.

Therefore, the effect of air on the PVK samples was investigated. The results are shown in **Figure 4.15**, which contains representative luminescence measurements of devices containing PVK that has been stored in different environments (Air vs $N_2$) for 3 days before finishing the device to additionally verify the effect of time on the PVK layer. The results are pretty clear as a very high luminance is still observed in both samples at appropriate voltages, with the Air stored sample even outperforming the Nitrogen stored sample which suggests that air storage does not negatively affect the quality of the PVK layer over the course of several days. It seems unexpected to see increased luminance values from old samples when compared to the reference values in **4.13** (bottom left), however in practice values approaching 10,000 cd/m$^2$ are not that rare for this system, which further highlights the poor luminance obtained from the AMOLF samples and the necessity of improvement.

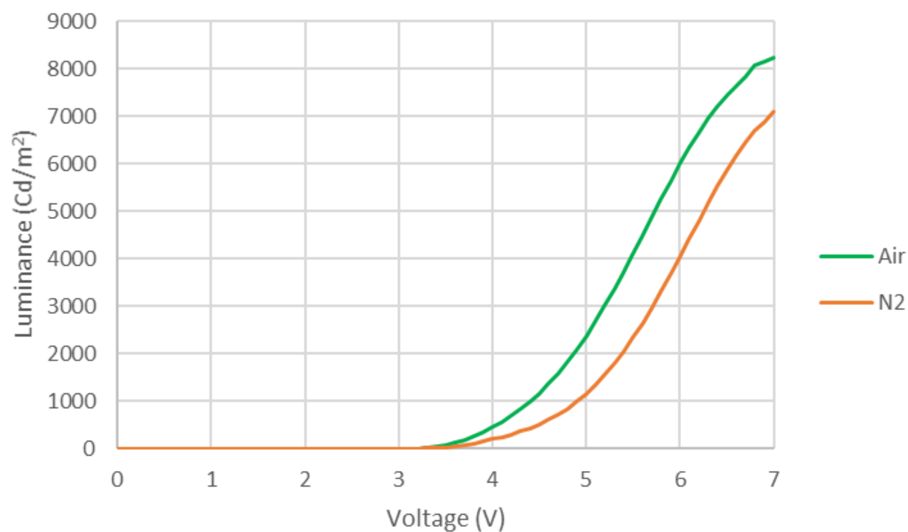


*Figure 4.15: Luminance (cd/m$^2$) over voltage of Cambridge reference devices left for 3 days after PVK deposition in Air (green) and nitrogen environments (orange) before finishing the device.*

As exposure to air or degradation over time has mostly been ruled out, this leaves the plasma treatments (either O2 or Ar+$CHF_3$) as the likely cause in hampering the device performance. As discussed in **Ch. 4.1.2**, the PVK morphology was investigated before and after plasma etching and little difference was observed. However, AFM does not provide conclusive data on the optoelectronic properties of a material and as such was only used to confirm the thickness and uniformity of the layer. It is very possible for the plasma to damage the PVK layer on a molecular level that would be difficult to identify with AFM measurements. However, the plasma treatments are necessary with the current SCIL protocol to ensure the proper adhesion of the sol-gel to the PVK layer (see **4.6** (bottom right) for the results where no plasma treatment is used) and to etch away residual sol-gel. Therefore, a change must be made to the protocol which removes the necessity for the plasma treatment, which will be the focus of the following chapter.

## 4.3 Device Stack Variation

The last chapter highlighted the possible problems involved with employing plasma etching steps on the organic HTL, which seems to have significantly hindered the final device performance. To fully circumvent the need of exposing PVK to any plasma treatment, a different device architecture was conceived. In this stack, the SCIL procedure is performed on the ITO directly before the PVK layer is spin-coated on top and ideally in between the sol-gel pattern (as shown in **Figure 4.16**). This would mean that both the O2 descum & sol-gel etching plasma treatment is performed on the ITO instead of the PVK layer which, as it is a stable metal oxide, is much more resistant to these types of plasma in comparison to an organic polymer. However, to achieve this new architecture 2 new steps need to be optimized in the procedure, namely the SCIL procedure on ITO & the PVK spin-coating procedure on the sol-gel pattern. Here the initial results are shown as a starting point for further optimizing the protocol.

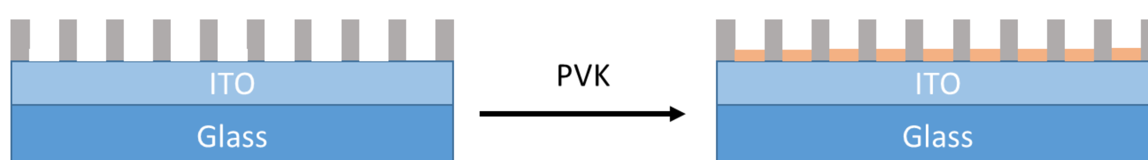


*Figure 4.16: A sideview layer diagram representing the alternate device architecture fabrication process.*

#### 4.3.1 SCIL on ITO

The first step in this new protocol is to verify the quality of the nano-hole pattern when the SCIL procedure is performed on the ITO substrate, as the adhesion of the sol-gel on the ITO might be different from the PVK and thus different surface preparation might be needed. The increased roughness of the ITO should not be a problem, as the sol-gel layer thickness (including the residual layer before plasma treatment) is significantly higher than the RMS roughness and the SCIL stamp has been shown to produce high quality patterns even on non-uniform surfaces [14]. Thus, the SCIL procedure was performed directly on ITO and investigated by AFM, the results of which are shown in **Figure 4.17**. It is important to note that there was a slight modification in the protocol, namely the standard plasma treatments were skipped, as the machinery to perform this was unavailable at the time. However, as the standard cleaning procedure of the ITO substrates already includes O2 plasma cleaning as a final step (albeit at a lower intensity but a significantly longer time), it was expected to not significantly affect the sol-gel adhesion, and the quality of the sol-gel pattern can still accurately be determined without etching away residual sol-gel.

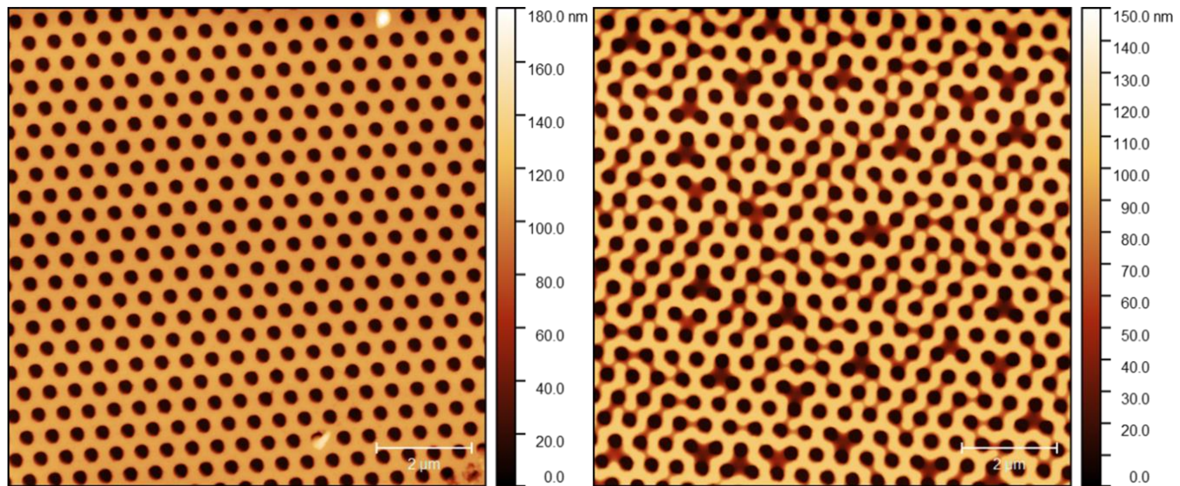


*Figure 4.17: Topographic AFM images sol-gel patterns fabricated on top of ITO.*

Initial AFM results seem promising, as **4.17** (left) displays the expected hexagonal hole array with a smooth top and bottom surface. Some defects are observed, which (partly) fill their respective holes. These are presumed to be either excess sol-gel aggregation or some other contamination. However, due to their low occurrence they are not seen as a significant problem for the overall pattern quality. What is more concerning are the areas which display a high and semi-patterned defect frequency consisting of triangular groups of holes that display decreased sol-gel height between them, and large networks of holes connected by lines consisting of a similar decrease in local sol-gel density (as seen in **4.17** (right)).

As these types of defect patterns have thus far not been observed in any SCIL patterning it is assumed to originate from some type of interaction with the ITO layer, possibly still originating from the change in plasma treatment procedure. However, as these high defect areas only show up sparingly over the substrate, they are ignored for now as they should not interfere significantly with the following PVK spincoating procedure. It is also important to note that the problems with the SCIL patterning, as discussed in **Ch. 4.1.3**, are still encountered but are just not highlighted in this chapter. All-in-all, the SCIL procedure seems similarly capable of fabricating high-quality nano-patterns on ITO as with PVK, although some new complications have arisen that still need to be addressed for future device manufacturing.

### 4.3.2 PVK on Sol-gel

The second step in this new protocol is probably the more ambitious of the 2, as it requires the homogeneous incorporation of the PVK layer into the nano-holes by spincoating. To achieve this, good control over spincoating parameters to ensure the proper distribution of the precursor solution over the surface and a strong affinity between the ITO present at the holes is needed. To this end, the plasma treatment protocol was essentially reversed. The patterned substrates were first subjected to a sol-gel etch as normal to expose the ITO at the bottom of the holes then the standard O2 plasma treatment was performed to increase the affinity of the PVK solution to ITO before it was spincoated.

It is unlikely for the previously optimized PVK spincoating protocol to produce adequate results due to the significantly altered surface conditions, both morphologically and chemically, on which the solution is deposited combined with the fact that the final layer thickness cannot be reduced by a succeeding O2 plasma treatment, as the whole goal of this new device architecture was to circumvent the usage of plasma etching on PVK. Therefore, various parameters will probably need to be varied consciously to identify the critical components for achieving a selectively uniform coating of the holes.

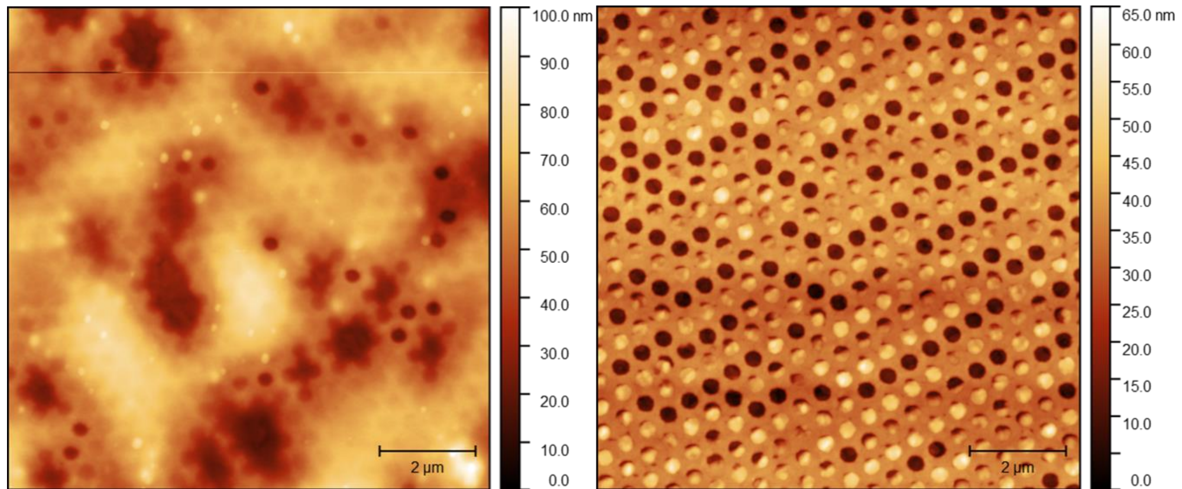


*Figure 4.18: Topographic AFM images of sol-gel patterns fabricated on top of ITO after PVK spincoating procedure at varying precursor concentrations. Left: 15 mg/mL, right: 5 mg/mL.*

A first step was made in this regard by varying the PVK concentration in the solution, as seen in the AFM results in **Figure 4.18** showing the results obtained from spin-coating with a standard (15mg/mL) and reduced (5 mg/mL) concentration. The reasoning behind the reduced concentration being that the total surface fraction that needs to be covered has significantly decreased by the existence of the nano-pattern on top of the fact that the PVK layer thickness obtained from the original procedure (20-25 nm) also needs to be reduced without the use of plasma etching.

A stark difference between the 2 figures is immediately apparent. **4.18** (left) shows a heavily aggregated PVK layer, which inhomogeneously but partly covers the hole-array with large accumulations of several 10s of nms in height, while some holes still seem fully exposed. In contrast to **4.18** (right), which shows an intact hole-pattern which displays an interesting alternating pattern with lines of seemingly unfilled holes next to lines of (partly) filled ones. The origin of this unexpected filling pattern is under debate; however it is likely some spin-coating effect causing some constructive and destructive interferences leading to such periodic filling. It is important to note that most of the seemingly unfilled holes are likely still partly covered in PVK as their depth is significantly shallower than expected (25 vs 65 nm), which suggest that a relatively thick (≈ 40 nm) layer is present. This suggests that the concentration could be reduced further to eventually arrive at a homogeneous thin covering as the large aggregations seem to disappear at lower concentrations. However, what is not represented in the AFM image is the fact that the surface is not fully covered with a PVK layer, as large distinct areas without any observable PVK are present that can be distinguished with the AFM's optical microscope and show a clean nano-pattern comparable with **4.17** (left) (only with reduced height due to the sol-gel etch).

Thus, not only the PVK thickness, but also the large-scale substrate coverage needs to be improved. Possible ways to achieve this in future work are to change the solvent to favor the deposition in the holes, vary the spincoating parameters to better suit a homogeneous coverage (such as higher RPM at an increased time for a better distribution over the substrate, and possibly a time-delay between drop-casting the solution and starting the spinning procedure to allow the PVK to settle within the holes), or prepare the surface in some way to improve the wetting of the PVK solution [35]. However, this goes beyond the scope of this project and is left for its possible future continuation. All in all, it can be concluded that an attempt was made to adapt the PVK thin film deposition protocol for selective incorporation into the nano-hole pattern with some amount of success. However, more work is needed to properly adapt the procedure for effective device fabrication in the future.

# 5. Conclusions & Outlook

## 5.1 Conclusion

The first part of this report aimed at providing an overview of various layers present within the device architecture, mostly dealing with their morphological features to make sure that a proper layer quality was achieved upon variation of the established protocol to adhere more closely to the recipe of Cambridge.

From these investigations, it can be concluded that an adequate coverage of the ITO substrate with PVK was achieved resulting in a thin (10-15 nm) layer with low RMS roughness (1-2 nm) despite the higher-than-expected roughness values of the underlying ITO (4-5 nm).

However, it became clear that this was not the case with respect to the nanopatterned sol-gel layer, as various defects in the nano-hole array ranging from missing individual holes, larger line defects (10s of μms) and even large areas without any patterning (100s of μms) were observed. Attempts were made to resolve this issue, however ultimately it was concluded that some damage to or contamination of the SCIL stamps were to blame. However, the patterned areas that were successfully produced were of high quality, with appropriate dimensions in comparison to the previously published results. Unfortunately, due to the limited time of this project, we were unable to produce a fully covering sol-gel pattern of satisfactory quality.

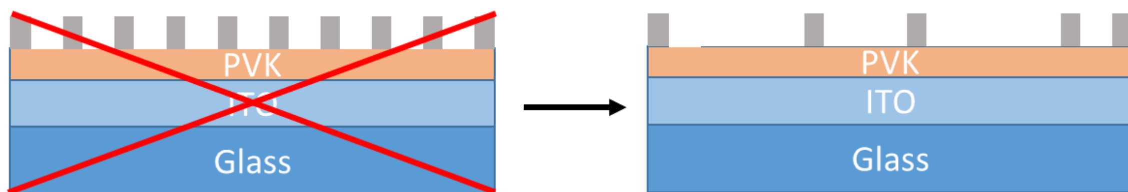


*Figure 5.1: A sideview layer diagram representing the problems associated with the patterning procedure.*

The following perovskite, ETL and top contact layers were mainly judged by the optoelectronic properties of the full device, as most of the protocol was kept identical to the properly functioning Cambridge reference devices. However, it was concluded that the perovskite coverage was directly linked to the sol-gel patterning quality as the perovskite incorporation seemed to favour the successfully patterned areas of the substrate. This gives another reason to improve the SCIL patterning in the future.

The second part of this report aimed to investigate the full device performance of the patterned devices in comparison to un-patterned versions fabricated at AMOLF and Cambridge. It became clear that the protocol at AMOLF was unable to produce adequately functioning LEDs, as the luminance of both patterned and unpatterned devices were 2 orders of magnitude lower compared to the Cambridge devices (10s vs 1000s of cd/m$^2$). As the only difference between the 2 reference devices is the PVK layer this was concluded to be the limiting factor. After verifying its stability in air over time (which is necessary to survive the trip to Cambridge), it was hypothesized that the $O_2$ plasma treatment was the cause of the stark difference in performance by damaging the PVK layer in some way. Unfortunately, this plasma treatment is a necessary step in the SCIL nanopatterning process. Therefore, it was concluded that a change in device architecture might be needed to obtain good LED performance.

The last part of this report was thus devoted to investigating the possibility of using a new device architecture, specifically one that flips the order in which the SCIL and PVK are performed to circumvent the use of plasma on the organic HTL. It was concluded that the SCIL procedure on ITO produced a pattern of comparable quality to earlier results reported in this project. However, the new PVK procedure which attempted to homogenously deposit a thin layer across the sol-gel nanopattern proved more challenging and significantly more optimization of the protocol is required to properly adapt it for effective device fabrication.

In summary, the results obtained from this project have made a step in the right direction towards achieving the proposed goal, which aimed to exhibit the enhanced and directional electroluminescent light emission of nanopatterned PeLEDs. However, due to unforeseen issues regarding the patterning procedure and quality of the HTL, more work is needed to properly optimize the device architecture in order to obtain a sufficient electroluminescent efficiency. Some possible next steps to this end will be discussed in the following chapter.

## 5.2 Outlook

Firstly, as mentioned in previous chapters, the overall pattern quality achieved by the SCIL procedure should be improved. As the current theory is that the stamp is damaged or contaminated in some way, it is vital to either clean or replace the current stamp. One known way to clean the stamp that has not been attempted yet is with HF, which can dissolve the sol-gel that is possibly attached to the pattern. However, working with HF requires special training due to the dangers it poses to humans and can additionally further damage the DMSO pattern. Therefore, it should only be done as a last attempt of cleaning the stamp. In any case, special attention should be paid to the stamp quality in the future and it would be beneficial to identify the exact cause of the damage/contamination.

It would also be interesting to properly verify the damage to the PVK layer by plasma treatment. This should be relatively straightforward, as the only difference from the established protocol would be the exemption of the plasma treatment step in the un-patterned devices, and it would back up the idea that the architecture of the device should be re-evaluated.

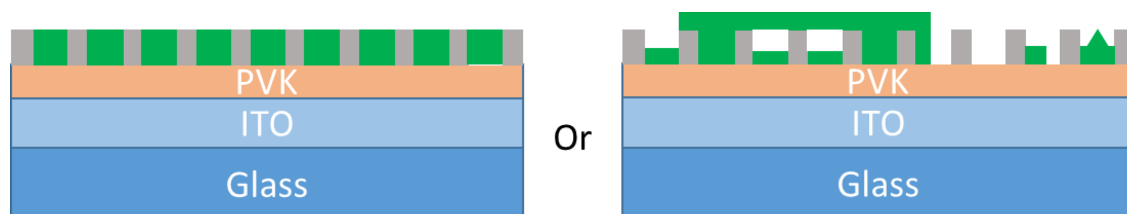


*Figure 5.2: A sideview layer diagram representing a few different ways in which the perovskite layer could fill the hole pattern.*

Another piece of missing information is the incorporation of the quasi-2D perovskite into the nanopatterns on the small-scale and its effect on the crystalline phase distribution, as up till now only crude observations of the crystallization have been made by eye (**Figure 5.2**).

Finally, we provide some suggestions for further variations in the device architecture that could improve the device performance in the future (as shown in **Figure 5.3**). The first idea is a stack on which the SCIL procedure is performed directly on glass, and both the ITO and PVK are then deposited within the hole pattern. This stems from the conclusion that the quality of the pre-deposited ITO layer might be limiting in some way as well, as Cambridge has observed an increase in performance when self-deposited ITO is used. The second idea features an additional HTL called Poly(4-butyl-N,N-diphenylaniline) (Poly-TPD) between the PVK and ITO layers, which has been shown to improve the band alignment between ITO and PVK [37]. Finally, one idea was to replace PVK with a self-assembled monolayer HTL called 2PACz, which would ideally be easier to incorporate into the hole-array [36].

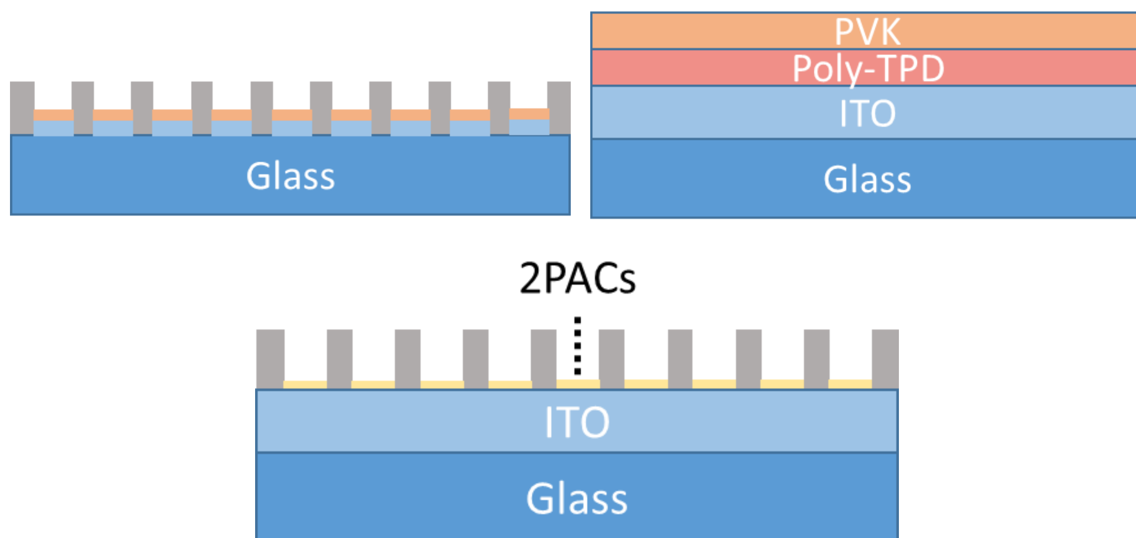


*Figure 5.3: A sideview layer diagram representing various other PeLED architectures that could possibly improve the device performance.*

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# A. Appendix

*Table A.1: An overview of spincoating protocols and PVK concentrations, including the resulting layer thicknesses before and after $O_2$ plasma procedure at varying times. Investigated using Profilometry*

| Spincoat protocol | PVK Concentration (mg/mL) | Thickness before etch (nm) | Etch time | Thickness after etch (nm) |
|---|---|---|---|---|
| AMOLF | 15 | ≈ 25-40 | 1:20 | Unclear |
| (2000 rpm, 1000 rpm/s, 45s) | | | 0:40 | ≈ 20-30 |
| | | | 0:20 | ≈ 30-35 |
| Cambridge | 5-9 | < 10 | X | X |
| (4000 rpm, 2000 rpm/s, 30s) | 10 | ≈ 10 | 1:20 | Unclear |
| | 11-14 | ≈ 10-15 | 1:20 | Unclear |
| | 15 | ≈ 15-25 | 1:20 | Unclear |

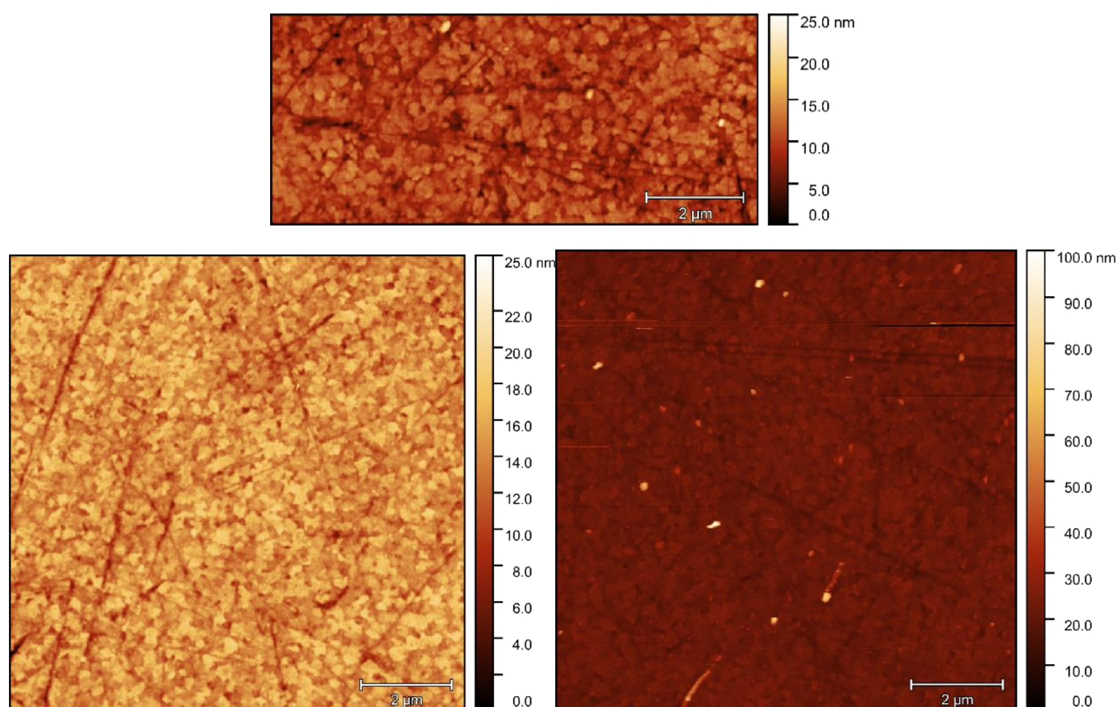


*Figure A.1: Uncorrected topographic AFM images of unetched (top), $O_2$ plasma treated (left) and $Ar+CHF_3$ plasma treated (right) PVK.*

*Figure A.2: A picture of patterned substrates after perovskite deposition. Substrates are observed under UV light to induce the photoluminescent emission observed.*